Sara Royuela

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Sara is a senior researcher in the Computer Sciences department at the Barcelona Supercomputer Center (BSC). She got her PhD in Computers Architecture from the Polytechnic University of Catalonia (UPC) with cum laude distinction in 2018. Sara is specialized in High Performance Computing (since 2010) and Real Time systems (since 2015). She has a vast experience on compilers and analysis tools for enhancing the productivity of parallel programming models, especially in systems constrained with real-time requirements. Sara has developed her communication skills by working in diverse heterogeneous research groups. Different experiences at teaching have helped her to develop critical thinking, and value empathy as a crucial characteristic for prosperity. Sara is a passionate and enthusiastic person that loves her work and enjoys sharing it with others.

Experience

2013 – CURRENTLY

Senior Researcher / Barcelona Supercomputing Center, BSC (Spain)

I'm currently working as a researcher in the Predictable Parallel Computing group at BSC. I co-direct several PhD and master students, while I continue and expand my research on parallel programming models, compiler analysis, and performance analysis tools.

I'm collaborating in several international projects, with different roles:

- H2020: *A Model-driven development framework for highly Parallel and EneRgy-Efficient computation supporting multi-criteria optimization, AMPERE* ↗. ('20-'22). I work as package leader in charge of code transformation and optimization techniques for performance, resiliency and heterogeneity.
- ESA: *High Performance Parallel Payload Processing for Space, HP4S* ('18-'20). I've been in charge of the technical developments to apply OpenMP in space missions. (A follow-up of this project is being prepared)
- H2020: *Edge and Cloud Computation: A Highly Distributed Software for Big Data Analytics, CLASS* ↗ ('18-'20). I was in charge of the initial setup of the project, by selecting and performing proof of concept on the technologies to be used for data distribution and parallel orchestration.

Researcher / Barcelona Supercomputing Center, BSC (Spain)

I worked as a PhD student in the Predictable Parallel Computing group at BSC. I focused my research on parallel programming models for safety-critical real-time systems. I participated in different international projects:

- FP7: *Parallel SOftware framework for time-CRitical mAny-core sysTEmS, PSOCRATES* ↗ ('13-'16).
- Bilateral: *Increasing the Guaranteed Performance in Many-core Heterogeneous Architectures*. ('16-'17).

2014 – 2016

Teacher / Salesians Sarrià (Spain)

I taught computer sciences courses to middle-level and upper-level training students.

2011 – 2013

Temporary Student Intern / Lawrence Livermore National Laboratory, LLNL (CA, USA)

I collaborated with the ROSE project group, in the Center for Applied Scientific Computing (CASC). I was in charge and developed tasks regarding compiler automatic transformations for OpenCL, support for OmpSs, and evaluation of different architectures (CPUs, GPUs i Intel's MIC).

2010 – 2011 / 2013-2015

Junior researcher / Barcelona Supercomputing Center, BSC (Spain)

I worked as master student first and junior researcher later, in the Programming Models group at BSC. I developed a static analysis compiler from the scratch for enhancing programmability and correctness in parallel programming models. I participated in different international projects:

- EU FP7 project: *ENabling technologies for a programmable many-CORE, ENCORE* ↗ ('10-'13).
- EU FP7 project: *Dynamical Exascale Entry Platform - Extended Reach, DEEP-ER* ↗ ('13-'15).

Education

JUNE 2018

PhD in Computer Architecture / Polytechnic University of Catalonia, UPC (Spain)

My thesis focuses on developing parallel programming models for distributed systems with high-performance and real-time requirements. It includes innovations in well-known parallel models from HPC, like OpenMP, and concurrent models from real-time computing, like Ada. I graduated with cum laude distinction.

JUNE 2015

Ms in Secondary School Training / Polytechnic University of Catalonia, UPC (Spain)

My thesis analyzes the use of ICTs and new learning-teaching techniques in Catalan schools, and implements a use case with upper-level training students that compares the master class and the inverted classroom.

JUNE 2011

Ms in Computer Architecture / Polytechnic University of Catalonia, UPC (Spain)

My thesis introduces new compiler analysis techniques for OpenMP and OmpSs to enhance the productivity and the correctness of the both parallel models. I was awarded for obtaining the third best academic results.

JUNE 2010

Informatics Engineering / Polytechnic University of Catalonia, UPC (Spain / France)

My final project developed of a tool to verify properties on systems modelled with Petri Nets applying lineal algebra instead of other common representations as trees or graphs, which cost is exponential.
I coursed six months in the École Politechnique de Nantes (France), under the ERASMUS program.

Scientific contributions

Research impact

The work I started during my PhD is having a great impact in the HPC and the Real Time communities. It has motivated and contributed towards (1) the introduction of functional safety and real-time aspects in the OpenMP standard via the collaboration with the OpenMP Language Committee, (2) the adoption of OpenMP in Ada via the collaboration with the Ada Rapporteur Group. It has also served to several students to develop their Bs degree, Ms degree and PhD theses.

I gather over 100 citations and have an h-index of 9. I have active collaborations with groups inside BSC, and groups at other institutions and companies such as Intel (Germany and USA), NVIDIA (USA), ISEP (Portugal), ETHZ (Zurich) and the LLNL (USA).

Publications

The most relevant publications of my career are the following:

- ***The AMPERE project: A model-driven development framework for highly parallel and energy-efficient computation supporting multi-criteria optimization.*** E. Quiñones, S. Royuela, et al. ISORC 2020.
- ***Enabling Ada and OpenMP runtimes interoperability through template-based execution***. S. Royuela, L.M. Pinho, and E. Quiñones. JSA 2020.
- ***A Functional Safety OpenMP* for Critical Real-Time Embedded Systems***. S. Royuela, A. Duran, M. A. Serrano, E. Quiñones, and X. Martorell. IWOMP 2017.
- ***Towards an OpenMP specification for critical real-time systems***. M.A. Serrano, S. Royuela, and E. Quiñones. IWOMP 2018.

- ***OpenMP tasking model for Ada: Safety and Correctnes***. S. Royuela, X. Martorell, E. Quiñones, and L.M. Pinho. AEiC 2017.
- ***A Lightweight OpenMP4 Run-time for Embedded Systems.*** R. E. Vargas, S. Royuela, M. A. Serrano, E. Quiñones, and X. Martorell. ASP-DAC 2016.
- ***Optimizing overlapped Memory Accesses in User-directed vectorization.*** D. Caballero, S. Royuela, R. Ferrer, A. Duran, and X. Martorell. ISC 2015.
- ***Compiler analysis for OpenMP tasks correctness.*** S. Royuela, R. Ferrer, D. Caballero, and X. Martorell. CF 2015.
- ***Auto-scoping for OpenMP Tasks.*** S. Royuela, A. Duran, C. Liao, and D. J. Quinlan. IWOMP 2012.

Other professional activities

International conferences and journals:

- I'm organizing a tutorial and a workshop in HiPEAC 2022.
- I've organized a tutorial in AEiC 2021.
- I've organized a panel in HILT 2020, resulting in a publication:
  - ***The OpenMP API for High Integrity Systems: Moving Responsibility from Users to Vendors***. M. Klemm, E. Quiñones, T. Taft, D. Ziegenbein, and S. Royuela. ACM SIGAda Ada Letters 2021.
- I've been program committee of C3PO 2020 and C3PO2021.
- I've served as technical reviewer in PACT 2018, TPDS 2018 and ICS 2013.
- I've been session chair in IWOMP 2018.

Education:

- I've been teacher assistant in the Parallelism course the Master CANS at UPC (2015).
- I've teach parallelism for real-time systems on the frame of Bojos per la Supercomputació (2019 – now).

Research:

- I've directed the one master thesis with cum laude distinction ↗. A Munera 2020. Publications:
  - ***Towards a qualifiable OpenMP framework for embedded systems***. A. Munera, S. Royuela, and E. Quiñones. DATE 2020
  - ***Techniques for reducing and bounding OpenMP dynamic memory***. A. Munera, S. Royuela, and E. Quiñones. BSC Doctoral Symposium 2019.
  - ***Poster: Techniques for reducing and bounding OpenMP dynamic memory***. A. Munera, S. Royuela, and E. Quiñones. ACACES Summer School 2019.
- I'm co-directing two PhD thesis:
  - A. Munera (yet to be enrolled). Publications:
    - ***Static analysis to enhance programmability and performance in OmpSs-2***. A. Munera, S. Royuela, R. Ferrer, R. Peñacoba, and E. Quiñones. ISC-HPC 2020 C3PO.
    - ***Experiences on the characterization of parallel applications in embedded systems with Extrae/Paraver***. A. Munera, S. Royuela, G. Llort, E. Mercadal, F. Wartel, and E. Quiñones. ICPP 2020.
  - C. Yu (third year). Publications:
    - ***Enhancing OpenMP tasking model: Performance and Portability***. C. Yu, S. Royuela, E. Quiñones. IWOMP 2021.
    - ***A Low Overhead Tasking Model for OpenMP***. C. Yu, S. Royuela, and E. Quiñones. Euro-Par 2021 PhD Symposium.
    - ***OpenMP to CUDA graphs: a compiler-based transformation to enhance the programmability of NVIDIA devices***. C. Yu, S. Royuela, and E. Quiñones. SCOPES 2020.
    - ***OpenMP static TDG runtime implementation and its usage in heterogeneous computing***. C. Yu, S. Royuela, and E. Quiñones. BSC Doctoral Symposium 2020.