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I. MAIN INFORMATION

I.1 Current Activity

Positions: Sr. Researcher, Computer Sciences, Barcelona Supercomputing Center (BSC), Spain (Sep. 2015).
Teaching and Research Staff, Universitat Politècnica de Catalunya (UPC), Spain (Jan. 2017).
Main responsibilities: Team Lead "Accelerators and Communications for HPC".
Manager of the BSC/UPC NVIDIA GPU Center of Excellence.
Member of the BSC Outreach Working Group.

I.2 Former Activity

Position: Postdoctoral Appointee.
Organization: Mathematics and Computer Science Division, Argonne National Laboratory (USA).
Main Responsibilities: Integrated into the core MPICH R&D team – derivatives **default MPI in 9 out of the top 10 supercomputers in TOP500**. Technical lead of the accelerator virtualization project (VOCL). Driving research area in system software for heterogeneous memories.
Dates: From Feb. 2013 to July 2015.

Position: Research Fellow and Research Assistant.
Organizations: Department of Computer Science and Engineering, Universitat Jaume I (Spain).
Department of Computer Engineering, Universitat Politècnica de València (Spain).
Main Responsibilities: Original Developer, Architect, and Development Supervisor of rCUDA.
Dates: Feb. 2009 – Feb. 2013.

I.3 Main Education

Title of Degree: PhD in Advanced Computer Systems.
PhD Title: Virtualization of Accelerators in High Performance Clusters.
Advisors: Rafael Mayo, Universitat Jaume I – Federico Silla, Universitat Politècnica de València (Spain).
University: Universitat Jaume I (Spain).
Grade: *Cum Laude.*
PhD Defense: Jan. 2013.
Impact: Extraordinary Doctoral Award – Derived in a spin-off (Remote Libraries).

Title of Degree: Advanced Studies Diploma (Post-graduate Diploma, MS equivalent).
Area: Advanced Computer Systems.
University: Universitat Jaume I (Spain).
Grade: A (9/10).
Date: Feb. 2010.

Title of Degree: Computer Engineering (5 years, BS + MS equivalent) – Specialization: Industrial Computers.
University: Universitat Jaume I (Spain).
Grade: A- (8.14/10 – 2.39/4).
Date: Jul. 2006.

I.4 Main Skills

Design and development of high-end runtime systems – High performance and cluster computing, accelerators
Programming model design and analysis – Low and high level programming (C, C++, Python, …)
Low-level HPC network programming and analysis – Team cooperation and coordination

I.5 Named Fellowships and Awards

I.5.1. Named Fellowships

1. Ramón y Cajal. Spanish Ministry of Science and Innovation. Ranked 2nd in category (score: 99.5/100, uccess rate: <8%). Highest named fellowship in Spain. Pre-selected Aug. 2021.
2. Ramón y Cajal. Spanish Ministry of Science and Innovation. Ranked 2nd in category (score: 99.5/100, uccess rate: <8%). Highest named fellowship for researchers in Spain. Pre-selected July 2020; Renounced (target institution not available on this edition).
3. Marie Sklodowska-Curie – Modality: Reintegration Panel (success rate: 12%). European Commission. "Advanced Ecosystem for Broad Heterogeneous Memory Usage" (ECO-H-MEM). Mar. 2018 – Feb. 2020.
4. Juan de la Cierva – Modality: Incorporation. Spanish Ministry of Economy, Industry, and Competitiveness. Ranked 2nd in category (score: 99/100, success rate: ~10%). After-postdoc fellowship. 2-year fellowship; Renounced to start Marie Sklodowska-Curie) Jan. 2017 – Feb. 2018.

I.5.2. Awards and Distinctions

1. Sr. Member, Association for Computing Machinery (ACM). Apr. 2021.
2. Impactful Paper. HiPC 25th Year Celebration. High Performance Computing Conference (HiPC), Hyderabad, India, Dec. 2018. (HiPC'11 paper selected to be among the 7 most impactful papers in HiPC's history).
3. BSC-CNS Annual Meeting Award. Dec. 2017.
4. 2017 IEEE TCHPC Award for Excellence for Early Career Researchers in High Performance Computing. Nov. 2017. (First European).
5. Extraordinary Doctoral Award. Universitat Jaume I (Spain). Sep. 2015.
6. Scale Challenge Finalist. The Eighth IEEE International Scalable Computing Challenge (SCALE), Shenzhen, China, May 2015.
7. Best Paper. The Fourth International Conference on Smart Grids, Green Communications and IT Energy-aware Technologies (ENERGY), Chamonix, France, Apr. 2014.
8. Best Technical Paper. IEEE International Conference on Cluster Computing (Cluster), Indianapolis, IN, USA, Sep. 2013.

I.6 Technology Transfer

1. The BSC/UPC NVIDIA GPU Center of Excellence incorporated a cuThomasBatch solver into the upcoming version of the cuSPARSE library of the NVIDIA Toolkit. 3.5 million downloads in 2017.
2. Contributions in MPICH grabbed by its multiple derivatives (such as Intel MPI, Cray MPI, IBM MPI, or ParaStation MPI), which are default in 9 out of the top 10 supercomputers in the TOP500 list.
3. Predoctoral research derived in a free binary package distributed by the Universitat Politècnica de València (Spain) and supported by a spin-off company (Remote Libraries).

I.7 Licensed/Registered Software

Title: Process-based Asynchronous Progress Model for MPI RMA (Casper).
Description: Portable and flexible process-based asynchronous progress model for MPI remote memory access (RMA) communication.
License: Open Source (BSD).
Authors: M. Si, A. J. Peña, and P. Balaji, Argonne National Laboratory.
IP Registry Code: OSS-15-1059 (registered May 2015).
Known Users: Intel Corporation.

Title: Extended Valgrind for Object-Differentiated Profiling (EVOP).
Description: Extensions to the Valgrind generic instrumentation framework and two of its tools to enable object-differentiated data-oriented profiling.
License: Open Source (GNU GPL).
Authors: A. J. Peña and P. Balaji, Argonne National Laboratory.
IP Registry Code: OSS-16-1096 (registered Mar. 2015; conferred Dec. 2015).
Known Users: Barcelona Supercomputing Center (BSC), Intel.

Title: New implementation of a GPU virtualization architecture – rCUDA.
Description: Enables the transparent use of GPUs placed in remote nodes through the CUDA API.
License: Free Sofware (binary).
Authors: J. Duato, R. Mayo, A. J. Peña, E. S. Quintana-Orti, and F. Silla.
Registered: Universitat Jaume I and Universitat Politècnica de València (Spain), May 2012.
Known Users: 500+. Exploited by a spin-off company.

Title: AstroAdapt
Description: Software tool to assist mobility-disabled people.
License: Open Source (GNU GPL), Jan. 2009.
Authors: A. Ortiz, T. Gallego, A. J. Peña, and L. Algarra, Universitat de València.
Known Users: Observatori Astronòmic, Universitat de València.

I.8 Professional Activity

Jan. 2017 – Current. Teaching and Research Staff, Universitat Politècnica de Catalunya, Spain.

Sep. 2015 – Current. Senior Researcher. Computer Sciences Department, Barcelona Supercomputing Center.

Feb. 2013 – July 2015. Postdoctoral Appointee. Mathematics and Computer Science Division, Argonne National Laboratory, USA.

Oct. 2012 – Feb. 2013. Research Fellow and Researcher. Department of Computer Science and Engineering, Universitat Jaume I, Spain.

Sep. 2011 – Dec. 2011. Graduate Intern. Swiss National Supercomputing Center, ETH Zürich, Switzerland.

Feb. 2009 – Sep. 2011 and Mar. 2012 – July 2012. Research Assistant. Department of Computer Engineering, Universitat Politècnica de València, Spain.

July 2007 – Oct. 2007. Research Fellow. Dept. of Computer Science and Engineering, Universitat Jaume I.

Nov. 2006 – July 2007, Feb. 2008 – July 2008, and Nov. 2008 – Dec. 2008. Collaborator, Collaboration Fellow, and Junior Research Assistant. Astronomical Observatory, Universitat de València, Spain.

July 2006 – Nov. 2006. Research Fellow. Department of Industrial Systems Engineering, Universitat Jaume I.

July 2005 – May 2006. Undergraduate Intern. Innova Advanced Consulting, Spain.

Feb. 2004 – July 2004. Collaboration Fellow. Department of Basic and Clinic Psychology and Psychobiology, Universitat Jaume I, Spain.

II. ACADEMIC ACTIVITY

II.1 Official University Teaching

1. Computer Structure (Labs). B.S. Computer Science. Univ. Politècnica de Catalunya, Spain. Since 2016

II.2 Advised PhD Theses

1. Kazuaki Matusumura. “Advancing the state of the art of directive-based programming for highly-heterogeneous supercomputers: runtime and compiler techniques”. Universitat Politècnica de Catalunya (Spain). Ongoing.

2. Sergio Iserte. “High-throughput computation through efficient resource management”. Universitat Jaume I (Spain). Nov. 2018. Excellent Cum Laude.
3. Adrián Castelló. “Unification of lightweight thread solutions and their application in high performance programming models”. Universitat Jaume I (Spain). Oct. 2018. Excellent Cum Laude.
4. Víctor García. “Memory hierarchies for future HPC architectures”. Universitat Politècnica de Catalunya (Spain). Oct. 2017. Excellent Cum Laude.

II.3 Advised Master Theses

1. Orestis Korakitis. “Towards supporting composability of directive-based programming models for heterogeneous computing”. Universitat Politècnica de Catalunya (Spain). July 2019. Qualif.: 9.5/10.
2. Ivan Martínez. “Simulating the behavior of the human brain on NVIDIA GPUs: cuHinesBatch & cuThomasBatch implementations”. Universitat Politècnica de Catalunya (Spain). Jan. 2018. Qualification: 9.5/10.
3. Aimar Rodríguez. “Design and development of support for GPU unified memory in OmpSs”. Universitat Politècnica de Catalunya (Spain). Oct. 2017. Qualification: 10/10.

II.4 Supervised Final Year Projects

1. August Boza. “Integration of GPU kernels with deep learning frameworks”. Universitat Politècnica de Catalunya (Spain). Oct. 2019.
2. Luis Toledo. “Design of a website for a cultural association”. Universitat Politècnica de València (Spain). Sep. 2012.
3. Tomás Navarro. “Implementation of rCUDA over VELO”. Universitat Politècnica de València (Spain). Sep. 2012.

II.5 Mentorships / Supervision

1. Pablo Izquierdo. Undergraduate Intern. Universidad de Cantabria, Spain. June 2021 – Aug. 2021.
2. Siddharth Rai. Postdoctoral Researcher. Barcelona Sueprcomputing Center. Jan. 2020 – Present.
3. Simon Garcia de Gonzalo. Postdoctoral Researcher. Barcelona Superc. Center. Nov. 2019 – Present.
4. Orestis Korakitis. Jr. Research Engineer. Barcelona Supercomputing Center. July 2020 – Present.
5. Guillermo Lloret. Jr. Research Engineer. Barcelona Supercomputing Center. Sep. 2019 – Sep. 2021.
6. Leonel Toledo. Postdoctoral Researcher. Bercelona Supercomputing Center. Aug. 2019 – Jan. 2021.
7. Perry Gibson. Summer Intern. The University of Edinburgh, UK. July 2019 – Aug. 2019.
8. Dimitris Voulgaris. Summer Intern. University of Thessaly, Greece. July 2019 – Aug. 2019.
9. Kazuaki Matsumura. PhD Student. Barcelona Supercomputing Center (BSC). July 2019 – Present.
10. Marc Jordà. Research Engineer. Barcelona Supercomputing Center (BSC). Jan. 2019 – Present.
11. Orestis Korakitis. MS Student. Barcelona Supercomputing Center. Oct. 2018 – June 2020.
12. Zheqi Yu. Summer Intern. University of Wolverhampton, UK. July 2018 – Aug. 2018.
13. Mohammad Owais. Jr. Research Engineer. Barcelona Supercomputing Center. Mar. 2018 – May 2019.
14. Kyunghun Kim. Research Engineer. Barcelona Supercomputing Center (Spain). May 2017 – July 2019
15. Pedro Valero-Lara. Researcher. Barcelona Supercomputing Center (Spain). Nov. 2016 – July 2019.
16. Ivan Martínez. Research Student. Barcelona Supercomputing Center (Spain). Sep. 2016 – Feb. 2018.
17. Aimar Rodríguez. Research Student. Barcelona Supercomputing Center (Spain). Apr. 2016 – Jul. 2018
18. Pau Farre. Jr. Engineer. Barcelona Supercomputing Center (Spain). Mar. 2016 – June 2018.
19. Marc Jordà. Jr. Engineer. Barcelona Supercomputing Center (Spain). Mar. 2016 – Dec. 2018.

20. Víctor García. Resident Student. Barcelona Supercomputing Center (Spain). Mar. 2016 – July 2017.
21. Min Si. Graduate Intern from The University of Tokyo (Japan). Argonne National Laboratory (USA). Apr. 2013 – Sep. 2013 and May 2014 – Apr. 2016.
22. Ashwin Aji. Graduate Student from Virginia Tech University (USA). Mar. 2014 – Nov. 2015.
23. Sayan Ghosh. Graduate Intern from The University of Houston (USA). Argonne National Laboratory (USA). May 2014 – June 2014.
24. Adrián Castelló. Graduate Student from Universitat Jaume I (Spain). Oct. 2014 – June 2015.
25. Xiuxia Zhang. Graduate Intern from Institute of Computing Technology, Chinese Academy of Sciences (China). Argonne National Laboratory (USA). June 2013 – May 2014.
26. Adrián Castelló. Research Scholar. Universitat Jaume I (Spain). May. 2011 – Feb. 2013.
27. Carlos Reaño. Research Assistant. Universitat Politècnica de València (Spain). Feb. 2011 – Feb. 2013.

II.6 Academic Committees

1. Predefense Committee Member. Albert Kahira. "Convergence of deep learning and high performance computing: Challenges and solutions". Universitat Politècnica de Catalunya (Spain). May 2021.
2. Referee, Competitive Promotion 2019, University of Luxembourg, 2019.
3. President, Predefese Committee. Sicong Zhuang. "Communication reduction techniques in numerical methods and deep neural networks". Universitat Politècnica de Catalunya (Spain). Sep. 2019.
4. Defense Committee Member. Antonio Lázaro. "Planificación dinámica de tareas en aceleradores". Universidad de Málaga (Spain). Mar. 2019.
5. Predefense Committee Member. Emilio Castillo. "Parallel architectures and runtime systems co-design for task-based programming models". Universtitat Politècnica de Catalunya (Spain). Dec. 2018.
6. Defense Committee Member. Guray Ozen. "Compiler and runtime based parallelization & optimization for CPUs". Universtitat Politècnica de Catalunya (Spain). Dec. 2018.
7. Defense Committee Member. Germán Ceballos. "Understanding task parallelism. Providing insight into scheduling, memory, and performance for CPUs and graphics". Uppsala University (Sweden). Dec. 2018.
8. Defense Committee Member. Enrique de Lucas Casamayor. "Reducing redundancy of real time computer graphics in mobile systems". Universitat Politècnica de Catalunya (Spain). Apr. 2018.
9. Predefense Committee Member. Francesc Josep Lordan Gomis. "Programming models for mobile environments". Universitat Politècnica de Catalunya (Spain). Feb. 2018.
10. Predefense Committee Member. Guray Ozen. "Compiler and runtime based parallelization & optimization for GPUs". Universitat Politècnica de Catalunya (Spain). Feb. 2018.
11. Predefense Committee Member. Ugljesa Milic. "Multicore architecture optimizations for HPC applications". Universitat Politècnica de Catalunya (Spain). July 2017.
12. Predefense Committee Member. Jan Ciesko. "On algorithmic reductions in task-parallel programming models". Universitat Politècnica de Catalunya (Spain). May 2017.
13. Defense Committee Member. Ivan Tanasiç. "Towards multiprogrammed GPUs". Universitat Politècnica de Catalunya (Spain). Feb. 2017.
14. Predefense Committee Member. Ivan Tanasiç. "Towards multiprogrammed GPUs". Universitat Politècnica de Catalunya (Spain). Nov. 2016.

II.7 Training

1. Professor Training Course (CAP). Statistics and Computer Science. Universitat Jaume I. Mar. 2008.

III. RESEARCH ACTIVITY

III.1 Participation in Projects

III.1.1 Principal Investigator

Title: Intel Sponsored Research Agreement. Enabling Homomorphically Encrypted Deep Learning Data and Models with Optane Technology.
Dates: Sep. 2019 – Aug. 2020.
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain.
Position: PI.
Funding: Private, Intel, $72,912.

Title: European joint Effort toward a Highly Productive Programming Environment for Heterogeneous Exascale Computing (EPEEC).
Dates: Oct. 2018 – Mar. 2022.
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain.
Position: Coordinator (Global PI, 10 partners).
Funding: Public, European Commission, 3,990,708.75€.

Title: Intel-BSC Exascale Laboratory. Statement of Work 5.1 on 3D XPoint Technology.
Dates: Oct. 2018 – Mar. 2021.
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain.
Position: PI.
Funding: Private, Intel, $500,000.

Title: Advanced Ecosystem for Broad Heterogeneous Memory Usage (ECO-H-MEM).
Dates: Mar. 2018 – Feb. 2020.
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain.
Position: Named Fellow. **Tutor:** Prof. Eduard Ayguadé.
Funding: Public, European Commission, 170,121.60€.

Title: BSC/UPC NVIDIA GPU Center of Excellence (GCoE).
Dates: Since Mar. 2016.
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain.
Position: Manager. **Director:** Prof. Mateo Valero.
Funding: Private, NVIDIA Co., 362,966.80€.

Title: Use of the Folding profiler to assist on data distribution for heterogeneous memory systems.
Dates: Sep. 2015 – Apr. 2018.
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain.
Position: PI.
Funding: Joint Laboratory for Exascale Computing (JLESC), 0€.

III.1.2 Other Leading Roles

Title: Mellanox – BSC SoW #1: Network Topologies, Network Profiling and Computation in Network
Main Responsibilities: Program Manager and Work Package Lead
Dates: Oct. 2021 – Sep. 2026
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain.
Position: Sr. Researcher **PI:** John D. Davis

Title: DEEP – Software for Exascale Architectures (DEEP-SEA)
Main Responsibilities: Task 3.2 "Memory Management" and Task 4.4 "HPC/HPDA Integration and Machine Learning"
Dates: Apr. 2021 – Mar. 2024
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain
Position: Sr. Researcher **PI:** Dr. Paul Carpenter

III.1.3 Participant Researcher

Title: The European PILOT
Main Responsibilities: Adapt automatic data distribution for heterogeneous memory systems framework.
Dates: Oct. 2021 – Sep. 2024.
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain.
Position: Senior Researcher. **PI:** John D. Davis.

Title: BSC-HUAWEI Research Agreement for HPC Technology Innovation Lab.
Main Responsibilities: Supervise R&D on accelerator design.
Dates: July. 2020 – June 2025.
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain.
Position: Senior Researcher. **PI:** John D. Davis.

Title: A Method and System for the Realisation of Exascale Computing in Europe (EuroEXA).
Main Responsibilities: Drive R&D on MPI communications for the Unimem architecture.
Dates: Sep. 2017 – Mar. 2021.
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain.
Position: Senior Researcher. **PI:** Dr. Paul Carpenter.

Title: European Exascale Processor & Memory Node Design (ExaNoDe).
Main Responsibilities: Drive R&D on MPI communications.
Dates: Jan. 2017 – Sep. 2018.
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain.
Position: Senior Researcher. **PI:** Dr. Paul Carpenter.

Title: Human Brain Project (HBP)
Main Responsibilities: Supervise R&D on GPU development.
Dates: Sep. 2016 – Mar. 2018.
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain.
Position: Senior Researcher. **PI:** Dr. Raül Sirvent.

Title: Intel-BSC Exascale Laboratory.
Main Responsibilities: R&D in data placement for heterogeneous memory systems.
Dates: Sep. 2015 – May 2018.
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain.
Position: Senior Researcher. **PI:** Prof. Jesús Labarta.

Title: Programming Model INTERoperability ToWards Exascale (INTERTWinE).
Main Responsibilities: R&D in MPI malleability.
Dates: Sep. 2015 – June 2017.
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain.
Position: Senior Researcher. **Responsible:** Prof. Xavier Martorell.

Title: Dynamical Exascale Entry Platform – Extended Research (DEEP-ER).
Main Responsibilities: R&D in fault-tolerance for the OmpSs offload feature.
Dates: Sep. 2015 – May 2017.
Organization: Computer Sciences Department, Barcelona Supercomputing Center, Spain.
Position: Senior Researcher. **Responsible:** Prof. Xavier Martorell.

Title: Exploring Efficient Data Movement Strategies for Exascale Systems with Deep Memory Hierarchies.
Main Responsibilities: To develop models for unified data movement among heterogeneous memory spaces.
Dates: Feb. 2013 – July 2015.
Organization: Mathematics and Computer Science Division, Argonne National Laboratory, USA.
Position: Postdoctoral Appointee. **Responsible:** Dr. Pavan Balaji.

Title: Energy-Aware Sustainable Computing on Future Technology–Paving the Road to Exascale Computing.
Main Responsibilities: Study the application and impact of the use of virtualized remote accelerators.
Dates: Jan. 2013 – Feb. 2013.
Organization: Department of Computer Science and Engineering, Universitat Jaume I, Spain.
Position: Researcher. **Responsible:** Prof. Enrique S. Quintana-Ortí.

Title: Real Data Center Cloud Services and Environment.
Main Responsibilities: Study of the adequateness and benefits of the application of the remote accelerators.
Dates: Nov. 2012 – Dec. 2012.
Organization: Department of Computer Science and Engineering, Universitat Jaume I, Spain.
Position: Researcher. **Responsible:** Dr. Rafael Mayo.

Title: Heterogeneous Computing Environments for High Performance Dense Linear Algebra on Dedicated Double Precision Hardware Accelerators.
Main Responsibilities: Study the application of the rCUDA software to the project.
Dates: Oct. 2012.
Organization: Department of Computer Science and Engineering, Universitat Jaume I, Spain.
Position: Research Fellow. **Responsible:** Prof. Enrique S. Quintana-Ortí.

Title: Server Architectures, Applications and Services (SAAS).
Main Responsibilities: Coordinate and supervise rCUDA development.
Dates: Mar. 2012 – July 2012.
Organization: Department of Computer Engineering (DISCA), Universitat Politècnica de València, **Spain.**
Position: Research Assistant. **Responsible:** Prof. José F. Duato.

Title: High Performance and High Productivity Computing (HP2C).
Main Responsibilities: Characterization of interaccelerator communication over HPC interconnects.
Dates: Sep. 2011 – Dec. 2011.
Organization: Swiss National Supercomputing Centre, ETH Zürich, Switzerland.
Position: Intern. **Supervisor:** Dr. Sadaf Alam.

Title: Extension of the Hypertransport Network Technology for the Enhancement of the Scalability of Internet Severs (PROMETEO/2008/060).
Main Responsibilities: Study of the viability of remotely-accelerated architectures as a means of reducing the number of accelerators in a cluster and achieving GPU/node decoupling. Responsible for development of the rCUDA project. Original developer and architect. Development Supervisor from 2011 to 2013.
Dates: Feb. 2009 – Sep. 2011.
Organization: Department of Computer Engineering (DISCA), Universitat Politècnica de València, Spain.
Position: Research Assistant. **Responsible:** Prof. José F. Duato.

Title: Astronomical Activities with Mobility-Disabled Persons.
Main Responsibilities: Co-design and development of software for people with mobile disability.
Dates: Nov. 2008 – Dec. 2008.
Organization: Astronomical Observatory, Universitat de València, Spain.
Position: Junior Research Assistant. **Responsible:** Dr. Amelia Ortiz.

Title: Remote Utilization of Robotic Telescopes and Astronomical Cameras on the Aras de los Olmos Observatory for Astronomy and Astrophysics Teaching.
Main Responsibilities: Design and development of a remote control telescope interface via Web (teaching-oriented). Automatization of all-sky image capturing process on wide-field cameras.
Dates: Feb. 2008 – July 2008.
Organization: Astronomical Observatory, Universitat de València, Spain.
Position: Collaboration Fellow. **Responsible:** Prof. Vicent J. Martínez.

Title: Integration of Information Technologies, Localization and Information for the Improvement of the Management Processes and Operations in the Road Freight Transport Sector.
Main Responsibilities: Design and development of communication software between onboard device and remote server. Built-in GPS data interpretation. Embedded operating system configuration.
Target Company: Castellón Business Association of Freight Transport (ACTM).
Dates: July 2007 – Oct. 2007.
Organization: Department of Computer Science and Engineering, Universitat Jaume I, Spain.
Position: Research Fellowship. **Responsible:** Dr. Germán Fabregat.

Title: Wide-Field Camera System for Optical Transitory Phenomena, Bolide & Meteor Observation & Study.
Main Responsibilities: Design / development of an automatic meteor detection algorithm on all-sky images.
Dates: Nov. 2006 – July 2007.
Organization: Astronomical Observatory, Universitat de València, Spain.
Position: Collaborator. **Responsible:** Prof. Juan Fabregat.

Title: Development of an Electronic Protection Relay.
Main Responsibilities: Development of system software and user application for the device, based on a DSP.
Target Company: Electrical Technology Institute (ITE).
Dates: July 2006 – Nov. 2006.
Organization: Department of Industrial Systems Engineering and Design, Universitat Jaume I, Spain.
Position: Research Fellow. **Responsible:** Dr. Enrique F. Belenguer.

III.2 Publications

* Main author **highlighted**; in papers as PhD student authors are ordered alphabetically and optionally by institution.

III.2.1. Citation Indices (Google Scholar)

Citations	h-index	i10-index	i100-index
1,640	21	35	3

III.2.2. International Journals

1. **G. Lloret-Talavera**, M. Jordà, H. Servat, F. Boemer, C. Chauhan, S. Tomishima, N. N. Shah, and A. J. Peña, "Enabling homomorphically encrypted inference for large DNN models", Transactions on Computers, IEEE, Apr. 2021. DOI: 10.1109/TC.2021.3076123. SJR Q1. (SJR 2020).
2. **S. Iserte**, R. Mayo, E. S. Quintana-Orti, and A. J. Peña, "DMRlib: Easy-coding and efficient resource management for job malleability", Transactions on Computers, IEEE, vol. 70, no. 9, Sep. 2021. DOI: 10.1109/TC.2020.3022933. SJR Q1. (SJR 2020).
3. **A. Castelló**, R. Mayo Gual, S. Seo, P. Balaji, E. S. Quintana-Orti, and A. J. Peña, "Analysis of threading libraries for high performance computing", Transactions on Computers, IEEE, vol. 69, no. 9, Sep. 2020. DOI: 10.1109/TC.2020.2970706. SJR Q1. (SJR 2020).
4. A. J. Peña and M. Si, "Guest editorial: Special Issue on Applications and System Software for Hybrid Exascale Systems", Parallel Computing, Elsevier, vol. 91, Mar. 2020. DOI: 10.1016/j.parco.2019.102583. SJR Q3.
5. **S. Iserte**, H. Martínez, S. Barrachina, M. Castillo, R. Mayo, and A. J. Peña, "Dynamic reconfiguration of noniterative scientific applications: A case study with HPG Aligner", The International Journal of High Performance Computing Applications (IJHPCA), SAGE, vol. 33, no. 5, pp. 804-816, Sep. 2019. DOI: 10.1177/1094342018802347. SJR Q2.
6. **K. Sala**, X. Teruel, J. M. Perez, A. J. Peña, V. Beltran, and J. Labarta, "Integrating blocking and non-blocking MPI primitives with task-based programming models", Parallel Computing, Elsevier, vol. 85, pp. 153-166, July 2019. DOI: 10.1016/j.parco.2018.12.008. SJR Q2.
7. **M. Jorda**, P. Valero-Lara, and A. J. Peña, "Performance evaluation of cuDNN convolution algorithms on NVIDIA Volta GPUs", Access, IEEE, vol. 7, pp. 70461-70473, May 2019. DOI: 10.1109/ACCESS.2019.2918851. SJR Q1.
8. **P. Valero-Lara**, R. Sirvent, A. J. Peña, J. Labarta, "MPI+OpenMP tasking scalability for multi-morphology simulations of the human brain", Parallel Computing, Elsevier, vol. 84, pp. 50-61, May 2019. DOI: 10.1016/j.parco.2019.03.006. SJR Q2.
9. **P. Valero-Lara**, I. Martínez-Pérez, R. Sirvent, X. Martorell, and A. J. Peña, "cuThomasBatch & cuThomasVBatch CUDA routines to compute batch of tridiagonal systems on NVIDIA GPUs", Concurrency and Computation: Practice and Experience, Wiley, vol. 30, no. 24, pp. 1-10, Dec. 2018. DOI: 10.1002/cpe.4909. SJR Q2.
10. **P. Valero-Lara**, I. Martínez-Pérez, R. Sirvent, A. J. Peña, X. Martorell, and J. Labarta, "Simulating the behavior of the human brain on GPUs", Oil & Gas Science and Technology - Revue d'IFP Energies Nouvelles, vol. 73, no. 63, pp. 1-15, Nov. 2018. DOI: 10.2516/ogst/2018061. SJR Q2.
11. **A. Castelló**, A. J. Peña, R. Mayo, J. Planas, E. S. Quintana-Ortí, and P. Balaji, "Exploring the interoperability of remote GPGPU virtualization using rCUDA and directive-based programming *models*", Journal of Supercomputing (JoS), Springer, vol. 74, no. 11, pp. 5628–5642, Nov. 2018. DOI: 10.1007/s11227-016-1791-y. SJR Q2.
12. **S. Iserte**, R. Mayo, E. S. Quintana-Orti, V. Beltran, and A. J. Peña, "DMR API: Improving cluster productivity by turning applications into malleable", Parallel Computing, Elsevier, vol. 78, pp. 54-66, Oct. 2018. DOI: 10.1016/j.parco.2018.07.006. SJR Q2.
13. **H. Servat**, J. Labarta, H. C. Hoppe, J. Giménez, and A. J. Peña, "Understanding memory access patterns using the BSC performance tools", Parallel Computing, Elsevier, vol. 78, pp. 1-14, Oct. 2018. DOI: 10.1016/j.parco.2018.06.007. SJR Q2.

14. **M. Si**, A. J. Peña, J. Hammond, P. Balaji, M. Takagi, Y. Ishikawa, "Dynamic adaptable asynchronous progress model for MPI RMA multiphase applications", Transactions on Parallel and Distributed Systems (TPDS), IEEE Comp. Society, vol. 29, no. 9, pp. 1975-1989, Sep. 2018. DOI: 10.1109/TPDS.2018.2815568. SJR Q1.
15. S. Chandrasekaran and A. J. Peña. "Special issue on applications for the heterogeneous computing era 2017", Parallel Computing, Elsevier, vol. 77, pp. 1-2, Sep. 2018. **Editorial.** DOI: 10.1016/j.parco.2018.06.002. SJR Q2.
16. **A. Castelló**, R. Mayo, K. Sala, V. Beltran, P. Balaji, and A. J. Peña, "On the adequacy of lightweight thread approaches for high-level parallel programming models", Future Generation Computer Systems (FGCS), Elsevier, vol. 84, pp. 22-31, Jul 2018. DOI: 10.1016/j.future.2018.02.016. SJR Q1.
17. S. Chandrasekaran and A. J. Peña. "Special issue on topics on heterogeneous computing", Parallel Comput, Elsevier, vol. 68, pp. 1-2, Oct. 2017. **Editorial.** DOI: 10.1016/j.parco.2017.08.001. SJR Q2.
18. **A. M. Aji**, A. J. Peña, P. Balaji, and W. Feng, "MultiCL: Enabling automatic scheduling for task-parallel workloads in OpenCL", Parallel Computing, Elsevier, vol. 58, pp. 37-55, Oct. 2016. DOI: 10.1016/j.parco.2016.05.006. SJR Q2.
19. **A. J. Peña** and P. Balaji, "A data-oriented profiler to assist in data partitioning and distribution for heterogeneous memory in HPC", Parallel Computing, Elsevier, vol. 51, pp. 46-55, Jan. 2016. DOI: 10.1016/j.parco.2015.10.006. SJR Q2.
20. **C. Reaño**, F. Silla, A. Castelló, A. J. Peña, R. Mayo, E. S. Quintana-Ortí, and J. Duato, "Improving the user experience of the rCUDA remote GPU virtualization framework", Concurrency and Computation: Practice and Experience (CCPE), Wiley, vol. 27, no. 14, pp. 3746-3770, Sep. 2015. DOI: 10.1002/cpe.3409. SJR Q2.
21. **A. J. Peña**, C. Reaño, F. Silla, R. Mayo, E. S. Quintana-Ortí, and J. Duato, "A complete and efficient CUDA-sharing solution for HPC clusters", Parallel Computing, Elsevier, vol. 40, no. 10, pp. 574-588, Dec. 2014. DOI: 10.1016/j.parco.2014.09.011. SJR Q1.

III.2.3. Indexed International Conferences

* Notice that conference papers are more valued than journal papers in our discipline; acceptance rates 15-30%.

1. **N. Guidotti**, P. Ceyrat, J. Barreto, J. Monteiro, R. Rodrigues, R. Fonseca, X. Martorell, and A. J. Peña, "Particle-in-cell simulation using asynchronous tasking", in *27th Int. European Conference on Parallel and Distributed Computing (Euro-Par)*, Lisbon, Portugal, Aug. 2021. GGS A-.
2. **L. Toledo**, P. Valero-Lara, S. Catalan, and A. J. Peña, "Tasking in accelerators performance evaluation", in *The 20th International Conference on Parallel and Distributed Computing, Applications and Technologies (PDCAT)*, Gold Coast, Australia, Dec. 2019. DOI: 10.1109/PDCAT46702.2019.00034. GGS B-.
3. **A. Farres**, C. Rosas, M. Hanzich, M. Jordà, and A. J. Peña, "Performance evaluation of fully anisotropic elastic wave propagation on NVIDIA Volta GPUs", in *81st EAGE Conference and Exhibition*. June 2019.
4. **P. Valero-Lara**, R. Sirvent, A. J. Peña, X. Martorell, and J. Labarta, "MPI+OpenMP tasking scalability for the simulation of the human brain", in *25th European MPI Users' Group Meeting (EuroMPI)*. Barcelona, Spain, Sep. 2018. DOI: 10.1145/3236367.3236373. CORE C.
5. **K. Sala**, J. Bellon, P. Farre, X. Teruel, J. M. Perez, A. J. Peña, D. Holmes, V. Beltran, and J. Labarta. "Improving the interoperability between MPI and task-based programming models", in *25th European MPI Users' Group Meeting (EuroMPI)*. Barcelona, Spain, Sep. 2018. DOI: 10.1145/3236367.3236382. CORE C.
6. **P. Valero-Lara**, I. Martinez-Perez, R. Sirvent, X. Martorell, and A. J. Peña, "NVIDIA GPUs scalability to solve multiple (batch) tridiagonal systems. Implementation of cuThomasBatch", in *12th International Conference on Parallel Processing and Applied Mathematics (PPAM)*, pp. 243-253, Lublin, Poland, Sep. 2017. DOI: 10.1007/978-3-319-78024-5_22. CORE C.
7. **H. Servat**, A. J. Peña, G. Llort, E. Mercadal, H. C. Hoppe, and J. Labarta, "Automating the application data placement in hybrid memory systems", in *IEEE International Conference on Cluster Computing (Cluster)*, pp. 126-136, USA, Sep. 2017. DOI: 10.1109/CLUSTER.2017.50. GGS A.

8. **A. Castelló**, S. Seo, R. Mayo, P. Balaji, E. S. Quintana-Orti, and A. J. Peña, "GLT: A unified API for lightweight thread libraries", in *23rd International European Conference on Parallel and Distributed Computing (Euro-Par)*, pp. 470-481, Santiago de Compostela, Spain, Aug. 2017. DOI: 10.1007/978-3-319-64203-1_34. GGS A-.
9. **V. Garcia-Flores**, E. Ayguade, and A. J. Peña, "Efficient data sharing on heterogeneous systems", in *The 46th International Conference on Parallel Processing (ICPP)*, pp. 121-130, Bristol, UK, Aug. 2017. DOI: 10.1109/ICPP.2017.21. GGS A-.
10. **A. Castelló**, S. Seo, R. Mayo, P. Balaji, E. S. Quintana-Orti, and A. J. Peña, "GLTO: On the adequacy of lightweight thread approaches for OpenMP implementations", *in The 46th International Conference on Parallel Processing (ICPP)*, pp. 60-69, Bristol, UK, Aug. 2017. DOI: 10.1109/ICPP.2017.15. GGS A-.
11. **A. J. Peña**, V. Beltran, C. Clauss, and T. Moschny, "Supporting automatic recovery in offloaded distributed programming models through MPI-3 techniques", in *International Conference on Supercomputing (ICS)*, pp. 1-10, Chicago, USA, Jun 2017. DOI: 10.1145/3079079.3079093. GGS A.
12. **P. Valero-Lara**, I. Martínez-Pérez, A. J. Peña, X. Martorell, R. Sirvent, and J. Labarta, "cuHinesBatch: Solving multiple Hines systems on GPUs. Human Brain Project", in *International Conference on Computational Science (ICCS)*, pp. 566-575, Zurich, Switzerland, June 2017. DOI: 10.1016/j.procs.2017.05.145. GGS B.
13. **J. Gómez-Luna**, I. El Hajj, L. Chang, V. Garcia-Flores, S. Garcia de Gonzalo, T. B. Jablin, A. J. Peña, and W. Hwu, "Chai: Collaborative heterogeneous applications for integrated-architectures", in *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pp. 1-11, San Francisco, USA, Apr. 2017. DOI: 10.1109/ISPASS.2017.7975269. GGS A-.
14. **V. Garcia**, J. Gomez-Luna, T. Grass, A. Rico, E. Ayguade, and A. J. Peña, "Evaluating the effect of last-level cache sharing on integrated GPU-CPU systems with heterogeneous applications", in *IEEE International Symposium on Workload Characterization (IISWC)*, pp. 1-10, Rhode Island, USA, Sep. 2016. DOI: 10.1109/IISWC.2016.7581277.
15. **A. Castelló**, A. J. Peña, S. Seo, R. Mayo, P. Balaji and E. S. Quintana-Orti, "A review of lightweight thread approaches for high performance computing", in *IEEE International Conference on Cluster Computing (Cluster)*, pp. 471-480, Taiwan, Sep. 2016. DOI: 10.1109/CLUSTER.2016.12. GGS A.
16. **S. Ghosh**, J. Hammond, A. J. Peña, P. Balaji, A. Gebremedhin, and B. Chapman, "One-sided interface for matrix operations using MPI-3 RMA: A case study with Elemental", in *International Conference on Parallel Processing (ICPP)*, pp. 1-10, Philadelphia, PA, USA, Aug. 2016. DOI: 10.1109/ICPP.2016.28. GGS A-.
17. **A. J. Peña**, W. Bland, and P. Balaji, "VOCL-FT: Introducing techniques for efficient soft error coprocessor recovery", in *The International Conference for High Performance Computing, Networking, Storage and Analysis (SC15)*, pp. 1-12, Austin, TX, USA, Nov. 2015. DOI: 10.1145/2807591.2807640. GGS A+.
18. **A. Aji**, A. J. Peña, P. Balaji, and W. Feng, "Automatic command queue scheduling for task-parallel workloads in OpenCL", in *IEEE International Conference on Cluster Computing (Cluster)*, pp. 42-51, Chicago, IL, USA, Sep. 2015. DOI: 10.1109/CLUSTER.2015.15. GGS A.
19. **A. Castelló**, A. J. Peña, R. Mayo, P. Balaji, and E. S. Quintana-Ortí, "Exploring the suitability of remote GPGPU virtualization for the OpenACC programming model using rCUDA", in *IEEE International Conference on Cluster Computing (Cluster)*, pp. 92-95, Chicago, IL, USA, Sep. 2015. DOI: 10.1109/CLUSTER.2015.23. GGS A.
20. **M. Si**, A. J. Peña, J. Hammond, P. Balaji, M. Takagi, and Y. Ishikawa, "Casper: An asynchronous progress model for MPI RMA on many-core architectures", in *29th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, pp. 665-676, Hyderabad, India, May 2015. DOI: 10.1109/IPDPS.2015.35. GGS A.
21. **M. Si**, A. J. Peña, J. Hammond, P. Balaji, and Y. Ishikawa, "Scaling NWChem with efficient and portable asynchronous communication in MPI RMA", in *The 15th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGrid)*, pp. 811-816, Shenzhen, China, May 2015. **Scale Challenge Finalist**. DOI: 10.1109/CCGrid.2015.48. GGS A.

22. **A. J. Peña** and P. Balaji, "Toward the efficient use of multiple explicitly managed memory subsystems", in *IEEE International Conference on Cluster Computing (Cluster)*, pp. 123-131, Madrid, Spain, Sep. 2014. DOI: 10.1109/CLUSTER.2014.6968756. GGS A.
23. **M. Si**, A. J. Peña, P. Balaji, M. Takagi, and Y. Ishikawa, "MT-MPI: Multithreaded MPI for many-core environments", in *ACM International Conference on Supercomputing (ICS)*, pp. 125-134, Munich, Germany, June 2014. DOI: 10.1145/2597652.2597658. GGS A.
24. **A. Castelló**, J. Duato, R. Mayo, A. J. Peña, E. S. Quintana-Ortí, V. Roca, and F. Silla, "On the use of remote GPUs and low-power processors for the acceleration of scientific applications", in *The Fourth International Conference on Smart Grids, Green Communications and IT Energy-aware Technologies (ENERGY)*, pp. 57-62, Chamonix, France, Apr. 2014. **Best Paper**.
25. **A. J. Peña**, R. G. Correa Carvalho, J. S. Dinan, P. Balaji, R. Thakur, and W. D. Gropp, "Analysis of topology-dependent MPI performance on Gemini networks", in *The 20th European MPI Users' Group Meeting (EuroMPI)*, pp. 61-66, Madrid, Spain, Sep. 2013. DOI: 10.1145/2488551.2488564. CORE C.
26. **C. Reaño**, F. Silla, R. Mayo, E. S. Quintana-Ortí, J. Duato, and A. J. Peña, "Influence of InfiniBand FDR on the performance of remote GPU virtualization", in *IEEE International Conference on Cluster Computing (Cluster)*, pp. 1-8, Indianapolis, IN, USA, Sep. 2013. **Best Technical Paper**. DOI: 10.1109/CLUSTER.2013.6702662. GGS A.
27. **A. J. Peña** and S. Alam, "Evaluation of inter- and intra-node data transfer efficiencies between GPU devices and their impact on scalable applications", in *The 13th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGrid)*, pp. 144-151, Delft, The Netherlands, May 2013. DOI: 10.1109/CCGrid.2013.15. GGS A.
28. **C. Reaño**, A. J. Peña, F. Silla, J. Duato, R. Mayo, and E. S. Quintana-Ortí, "CU2rCU: Towards the complete rCUDA remote GPU virtualization and sharing solution", in *Proceedings of the International Conference on High Performance Computing (HiPC)*, pp. 1-10, Pune, India, Dec. 2012. DOI: 10.1109/HiPC.2012.6507485. GGS B.
29. **S. Alam**, J. Poznanovic, U. Varetto, N. Bianchi, A. J. Peña, and N. Suvanphim, "Early experiences with the Cray XK6 hybrid CPU and GPU MPP platform", in *Cray User Group Conference (CUG)*, pp. 1-10, Stuttgart, Germany, Apr. 2012.
30. J. Duato, **A. J. Peña**, F. Silla, J. C. Fernández, R. Mayo, and E. S. Quintana-Orti, "Enabling CUDA acceleration within virtual machines using rCUDA", in *High Performance Computing Conference (HiPC)*, pp. 1-10, Bangalore, India, Dec. 2011. **HiPC Impactful Paper**. DOI: 10.1109/HiPC.2011.6152718. GGS B.
31. J. Duato, R. Mayo, **A. J. Peña**, E. S. Quintana-Ortí, and F. Silla, "Performance of CUDA virtualized remote GPUs in high performance clusters", in *International Conference on Parallel Processing (ICPP)*, pp. 365-374, Taipei, Taiwan, Sep. 2011. DOI: 10.1109/ICPP.2011.58. GGS A.

III.2.4. International Workshops

1. **S. Rivas-Gomez**, A. J. Peña, D. Moloney, E. Laure, and S. Markidis, "Exploring the Vision Processing Unit as co-processor for inference", in *The Eighth International Workshop on Accelerators and Hybrid Exascale Systems (AsHES)*, pp. 1-10, Vancouver, Canada, May 2018.
2. **M. Jordà**, P. Valero-Lara, and A. J. Peña, "Convolutional deep learning (cuDNN) on NVIDIA GPUs", in *International Workshop on Optimization and Learning: Challenges and Applications (OLA)*, pp. 1-2, Alicante, Spain, Feb. 2018.
3. **S. Iserte**, R. Mayo, E. S. Quintana-Orti, V. Beltran, and A. J. Peña, "Efficient scalable computing through flexible applications and adaptive workloads", in *Tenth International Workshop on Parallel Programming Models and Systems Software for High-End Computing (P2S2)*, pp. 180-189, Bristol, UK, Aug. 2017. DOI: 10.1109/ICPPW.2017.36.
4. **H. Servat**, J. Labarta, H. C. Hoppe, J. Gimenez, and A. J. Peña, "Integrating memory perspective into the BSC performance tools", in *Tenth International Workshop on Parallel Programming Models and Systems Software for High-End Computing (P2S2)*, pp. 231-232, Bristol, UK, Aug. 2017. DOI: 10.1109/ICPPW.2017.42.

5. **S. Iserte**, A. J. Peña, R. Mayo, E. S. Quintana-Ortí, and V. Beltrán, "Dynamic management of resource allocation for OmpSs jobs", pp. 55-58, in *PhD Symposium on Sustainable Ultrascale Computing Systems (NESUS PhD)*, Timisoara, Romania, Feb. 2016.
6. **A. J. Peña** and P. Balaji, "A framework for tracking memory accesses in scientific applications", in *43nd International Conference on Parallel Processing Workshops (ICPP-W)*, pp. 235-244, Minneapolis, MN, USA, Sep. 2014. DOI: 10.1109/ICPPW.2014.40.
7. J. Duato, **A. J. Peña**, F. Silla, R. Mayo, and E. S. Quintana-Ortí, "rCUDA: Reducing the number of GPU-based accelerators in high performance clusters", in *Proceedings of the International Conference on High Performance Computing and Simulation (HPCS)*, pp. 224-231, Caen, France, June 2010. DOI: 10.1109/HPCS.2010.5547126. 200+ citations.
8. J. Duato, F. D. Igual, R. Mayo, **A. J. Peña**, E. S. Quintana-Ortí, and F. Silla, "An efficient implementation of GPU virtualization in high performance clusters", in *Euro-Par 2009, Parallel Processing – Workshops***,** 6043, pp. 385-394, Lecture Notes in Computer Science, Springer, 2010. DOI: 10.1007/978-3-642-14122-5_44.
9. M. F. Dolz, J. C. Fernández, E. S. Quintana-Ortí, R. Mayo, and A. J. Peña, "Research line on power-aware computing by the High Performance and Architectures Group", in *COST Action IC0804 on Energy Efficiency in Large Scale Distributed Systems*, pp. 32-36, Toulouse, France, Nov. 2009.

III.2.5. International Posters

1. **A. J. Peña**, "EPEEC: Productivity at exascale", in *ISC High Performance*, Germany, June 2019.
2. **K. Kim**, A. J. Peña, P. Carpenter, P. Petrakis, M. Ploumidis, M. Marazakis, Y. Guo, K. Raffenetti, and P. Balaji, "Toward developing a Unimem OFI provider for MPI support", in *25th European MPI Users' Group Meeting (EuroMPI)*, Barcelona, Spain, Sep. 2018.
3. **S. Iserte**. H. Martinez, S. Barrachina, M. Castillo, R. Mayo, E. S. Quintana-Orti, and A. J. Peña, "MPI malleability integration into a bioinformatics tool", in *25th European MPI Users' Group Meeting (EuroMPI)*, Barcelona, Spain, Sep. 2018.
4. **P. Valero-Lara**, I. Martinez-Perez, A. J. Peña, X. Martorell, R. Sirvent, and J. Labarta, "Simulating the behavior of the human brain on NVIDIA GPUs (Human Brain Project)", in *GPU Technology Conference (GTC)*, Silicon Valley, USA, May 2017.
5. **V. García**, J. Gómez-Luna, T. Grass, A. Rico, A. J. Peña, and E. Ayguadé, "Analyzing the effect of last level cache sharing on integrated platforms with fine-grain CPU-GPU collaboration", in *GPU Technology Conference Europe (GTC Europe)*, Amsterdam, The Netherlands, Sep. 2016.
6. **A. Castelló**, A. J. Peña, S. Seo, R. Mayo, P. Balaji, and E. S. Quintana-Ortí, "On the use of lightweight threads", in *Advanced Computer Architectures and Compilation for Embedded Systems (ACACES)*, pp. 83-86, HiPEAC Network of Excellence, Fuggi, Italy, July 2016.
7. **A. J. Peña** and P. Balaji, "Understanding data access patterns using object-differentiated memory profiling", in *The 15th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGrid)*, pp. 1143-1146, Shenzhen, China, May 2015. DOI: 10.1109/CCGrid.2015.42.
8. **K. Raffenetti**, A. J. Peña, and P. Balaji, "Toward implementing robust support for Portals 4 networks in MPICH", in *The 15th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGrid)*, pp. 1173-1176, Shenzhen, China, May 2015. DOI: 10.1109/CCGrid.2015.79.
9. **C. Reaño**, F. Silla, A. J. Peña, G. Shainer, S. Schultz, A. Castelló, E. S. Quintana-Ortí, and J. Duato, "Boosting the performance of remote GPU virtualization using InfiniBand Connect-IB and PCIe 3.0", in *IEEE International Conference on Cluster Computing* (*Cluster)*, pp. 266-267, Madrid, Spain, Sep. 2014. DOI: 10.1109/CLUSTER.2014.6968737.
10. J. Duato, **A. J. Peña**, F. Silla, R. Mayo, and E. S. Quintana-Ortí, "rCUDA InfiniBand performance", in *International Supercomputing Conference (ISC)*, Hamburg, Germany, June 2011.
11. J. Duato, R. Mayo, **A. J. Peña**, E. S. Quintana-Ortí, and F. Silla. "Network influence on rCUDA", in *Advanced Computer Architectures and Compilation for Embedded Systems (ACACES)*, pp. 9-12, HiPEAC Network of Excellence, Terrassa (Barcelona), Spain, July 2010.
12. J. Duato, F. D. Igual, R. Mayo, **A. J. Peña**, E. S. Quintana-Ortí, and F. Silla, "Virtualized remote GPUs", in *Advanced Computer Architectures and Compilation for Embedded Systems (ACACES)*, pp. 221-224, HiPEAC Network of Excellence, Terrassa (Barcelona), Spain, July 2009.

13. **A. J. Peña** and J. Fabregat, "A robust bolid and fireball detection algorithm for all-sky sequential images", in *Meteoroids*, pp. 24-25, Barcelona, Spain, June 2007.

III.2.6. International Oral Communications

1. A. J. Peña, "EPEEC: Productivity at Exascale", in *Communications of the ACM Europe Region Special Section Virtual Workshop*, Virtual, Aug. 2021.
2. **K. Matsumura**, S. Garcia de Gonzalo and A. J. Peña, "Wrapping up existing OpenACC compilers for runtime extension", in PhD Forum, *ISC High Performance*, Virtual, June 2021.
3. **G. Lloret-Talavera**, M. Jordà, H. Servat, F. Boemer, C. Chauhan, S. Tomishima, N. N. Shah, and A. J. Peña (BSC), "Optane PMem as an enabler for large DNN models with homomorphic encryption", in *2nd Workshop on Heterogeneous Memory Systems (HMEM)*, Virtual, June 2021.
4. **L. Toledo**, P. Valero-Lara, and A. J. Peña, "Accelerating machine learning applications using CUDA Graph and OpenACC", in *GPU Technology Conference*, Virtual, Apr. 2021.
5. A. J. Peña, "Results and lessons learned by EPEEC", in *PROHEXA: Programming environments and models for improved productivity for heterogeneous Exascale Computing Systems* Workshop, Virtual, Jan. 2021.
6. A. J. Peña, "Overview of EPEEC: European joint Effort toward a Highly Productive Programming Environment for Heterogeneous Exascale Computing", in *PROHEXA: Programming environments and models for improved productivity for heterogeneous Exascale Computing Systems* Workshop, Virtual, Jan. 2021.
7. **G. Lloret-Talavera**, M. Jorda, H. Servat, F. Boemer, C. Chauhan, S. Tomishima, N. N. Shah, and A. J. Peña, "Optane PMem as an enabler for large DNN models with homomorphic encryption", in *Intel Extreme Performance Users Group (IXPUG) Annual Conference*, Virtual, Oct. 2020.
8. A. J. Peña, "A software ecosystem to save money in DRAM and increase performance with Optane DIMMs", in *Intel HPC + AI Pavilion*, Virtual, June 2020.
9. **M. Jordà**, H. Servat, J. Labarta, and A. J. Peña, "Easing the use of Optane DIMMs as part of heterogeneous memory systems", in *Intel HPC Developer Conference*, Denver, CO, USA, Nov. 2019.
10. **M. Jordà**, H. Servat, and A. J. Peña, "Toward easing the use of Optane DIMMs as part of heterogeneous memory systems", in *Intel Extreme Performance Users Group (IXPUG) Annual Conference*, Geneva, Switzerland. Sep. 2019.
11. **M. Jordà**, P. Valero-Lara, an A. J. Peña, "Improved convolution implementations on NVIDIA GPUs", in 9*th Joint Laboratory for Extreme-Scale Computing Workshop (JLESC)*, Knoxville, USA, Apr. 2018.
12. **P. Valero-Lara** and A. J. Peña, "Filling the performance gap in convolution implementations for NVIDIA GPUs", in *GPU Technology Conference (GTC)*, Silicon Valley, USA. Mar. 2019.
13. A. J. Peña, "Collaboration opportunities with the Accelerators and Communications for HPC Team at BSC", in 8*th Joint Laboratory for Extreme-Scale Computing Workshop (JLESC)*, Barcelona, Spain, Apr. 2018.
14. **A. J. Peña** *et. al.*, "Use of the Folding profiler to assist on data distribution for heterogeneous memory systems", in 8*th Joint Laboratory for Extreme-Scale Computing Workshop (JLESC)*, Barcelona, Spain, Apr. 2018.
15. A. J. Peña, "MultiGPU made easy by OmpSs + CUDA/OpenACC", in *GPU Technology Conference (GTC)*, Silicon Valley, USA. Mar. 2018.
16. **P. Valero-Lara**, I. Martínez-Pérez, A. J. Peña, X. Martorell, R. Sirvent, and J. Labarta. "cuHinesBatch: Solving multiple Hines systems on GPUs", in *2nd HBP Student Conference (HBPSC)*, Ljubljana, Slovenia, Feb. 2018.
17. A. J. Peña and F. Mantovani, "Automatic frequency scaling for embedded co-processor acceleration", in *Workshop on Heterogeneous and Low-Power Data Center technologies (HELP-DC)*, Manchester, UK, Jan. 2018.
18. **A. J. Peña**, H. Servat, *et. al.*, "Use of the Folding profiler to assist on data distribution for heterogeneous memory systems", in *7th Joint Laboratory for Extreme-Scale Computing Workshop (JLESC)*, Urbana, USA, June 2017.

19. **A. J. Peña**, H. Servat, G. Llort, J. Giménez, J. Labarta, "Use of the Folding profiler to assist on data distribution for heterogeneous memory systems", in *6th Joint Laboratory for Extreme-Scale Computing Workshop (JLESC),* Kobe, Japan, Dec. 2016.
20. **A. J. Peña** and L. Oden, "Data distribution approaches for heterogeneous memory systems", in *5th Joint Laboratory for Extreme-Scale Computing Workshop (JLESC)*, Lyon, France, June 2016.
21. **A. J. Peña** and H. Servat, "Data placement on heterogeneous memory systems in HPC", in *4th Joint Laboratory for Extreme-Scale Computing Workshop (JLESC),* Bonn, Germany, Nov. 2015.
22. **H. Servat** and A. J. Peña, "Study the use of the Folding hardware-based profiler to assist on data distribution for heterogeneous memory systems in HPC", in *3rd Joint Laboratory for Extreme-Scale Computing Workshop (JLESC),* Barcelona, Spain, June 2015.
23. A. J. Peña. "Toward heterogeneous memory systems for HPC", in Enhancing Software Development for Emerging Platforms Using Algorithms and Performance Tools Minisymposium, SIAM CSE, Salt Lake City, UT, USA, Mar. 2015.
24. **A. J. Peña** and P. Balaji. "The upcoming era of memory heterogeneity in compute nodes", in *2nd Joint Laboratory for Extreme-Scale Computing Workshop (JLESC)*, Chicago, IL, USA, Nov. 2014.
25. A. J. Peña, "Virtualization of accelerators in high performance clusters", in *The International Conference for High Performance Computing, Networking, Storage and Analysis (SC)*, Dissertation Research Showcase, Salt Lake City, UT, USA, Nov. 2012.
26. J. Duato, **A. J. Peña**, F. Silla, R. Mayo, and E. S. Quintana-Ortí, "Modeling the CUDA remoting virtualization behaviour in high performance networks", in *Workshop on Language, Compiler, and Architecture Support for GPGPU (LCA-GPGPU-I)*, Bangalore, India, Jan. 2010.

III.2.7. Spanish Conferences

1. **A. Castelló**, R. Mayo, S. Seo, P. Balaji, E. S. Quintana-Ortí, and A. J. Peña, "GLTO: Una implementación de OpenMP sobre hilos ligeros", in *XXIX Jornadas de Paralelismo*, Teruel, Spain, Sep. 2018. DOI: 10.5281/zenodo.1413157.
2. **S. Iserte**, R. Mayo, E. S. Quintana-Orti, V. Beltran, and A. J. Peña, "El camino desde la maleabilidad MPI hasta las cargas de trabajos adaptativas", in *XXVIII Jornadas de Paralelismo*, pp. 1-6, Malaga, Spain, Sep. 2017. DOI: 10.5281/zenodo.999424.
3. **A. Castelló**, J. Duato, R. Mayo, A. J. Peña, and E. S. Quintana-Ortí, "Acelerando aplicaciones científicas con GPUs remotas y procesadores de bajo consumo", in *XXV Jornadas de Paralelismo*, pp. 1-7, Valladolid, Spain, Sep. 2014.
4. **S. Iserte**, A. Castelló, A. J. Peña, C. Reaño, J. Prades, F. Silla, R. Mayo, E. S. Quintana-Ortí, and J. Duato, "Extendiendo SLURM con soporte para el uso de GPUs remotas", in *XXV Jornadas de Paralelismo*, pp. 1-9, Valladolid, Spain, Sep. 2014.
5. **C. Reaño**, A. Castelló, S. Iserte, A. J. Peña, F. Silla, R. Mayo, E. S. Quintana-Ortí, and J. Duato, "Virtualización remota de GPUs: Evaluación de soluciones disponibles para CUDA", in *XXIV Jornadas de Paralelismo*, pp. 1-6, Madrid, Spain, Sep. 2013.
6. **S. Iserte**, A. Castelló, C. Reaño, A. J. Peña, F. Silla, R. Mayo, E. S. Quintana-Ortí, and J. Duato, "Un planificador de GPUs remotas en clusters HPC", in *XXIV Jornadas de Paralelismo*, pp. 1-6, Madrid, Spain, Sep. 2013.
7. **C. Reaño**, A. J. Peña, F. Silla, J. Duato, R. Mayo, and E. S. Quintana-Ortí, "CU2rCU: A CUDA-to-rCUDA converter", in *XXIII Jornadas de Paralelismo*, pp. 44-49. Elche, Spain, Sep. 2012.
8. J. Duato, **A. J. Peña**, F. Silla, J. C. Fernández, R. Mayo, and E. S. Quintana-Ortí, "A new approach to rCUDA", in *XXII Jornadas de Paralelismo*, pp. 305-310, La Laguna, Spain, Sep. 2011.
9. **C. Reaño**, A. J. Peña, F. Silla, R. Mayo, E. S. Quintana-Orti, and J. Duato, "rCUDA: Uso concurrente de dispositivos compatibles con CUDA de forma remota. Adaptación a CUDA 4", in *XXII Jornadas de Paralelismo*, pp. 311-316, La Laguna, Spain, Sep. 2011.
10. J. Duato, **A. J. Peña**, F. Silla, R. Mayo, and E. S. Quintana-Ortí, "rCUDA: A framework to perform remote CUDA calls", in *XXI Jornadas de Paralelismo*, pp. 519-526, Valencia, Spain, Sep. 2010.
11. J. Duato, F. D. Igual, R. Mayo, **A. J. Peña**, E. S. Quintana-Ortí, and F. Silla, "CUDA remoto para clusters de altas prestaciones", in *II Workshop en Aplicaciones de Nuevas Arquitecturas de Consumo y Altas Prestaciones (ANACAP),* pp. 1-6, Móstoles (Madrid), Spain, Nov. 2009.

12. J. Duato, **A. J. Peña**, F. Silla, F. D. Igual, R. Mayo, and E. S. Quintana-Ortí, "Accelerating computing through virtualized remote GPUs", in *XX Jornadas de Paralelismo*, pp. 635-639, A Coruña, Spain, Sep. 2009.
13. **A. J. Peña**, J. M. Claver, A. Sanjuan, and V. Arnau, "Análisis paralelo de secuencias de ADN mediante el uso de GPU y CUDA", in *Workshop de Aplicaciones de Nuevas Arquitecturas de Consumo y Altas Prestaciones (ANACAP)*, pp. 1-6, Móstoles (Madrid), Spain, Nov. 2008.
14. **R. Rodríguez**, J. M. Claver, G. Fernández, A. J. Peña, and J. L. Sánchez, "Aceleración de la estimación de movimiento en la codificación H.264/AVC mediante GPUs", in *Workshop de Aplicaciones de Nuevas Arquitecturas de Consumo y Altas Prestaciones (ANACAP)*, pp. 1-6, Móstoles (Madrid), Spain, Nov. 2008.

III.3 Invited Talks

III.3.1. Keynotes

1. "Using heterogeneous memory systems". *Córdoba HiPerNav Week*, Córdoba, Spain. Sep. 2018.
2. "The heterogeneity challenge", in *Heterogeneity Alliance: Better Together, HiPEAC 2018 Conference*, Manchester, UK, Jan. 2018.
3. "The Nightmare and Power of Heterogeneity in HPC", in *Tenth International Workshop on Parallel Programming Models and Systems Software for High-End Computing (P2S2)*, Bristol, UK, Aug. 2017.

III.3.2. Panels

1. "PROCESS Panel", in *Workshop on Platform-driven e-infrastructure innovations*, Amsterdam, The Netherlands, Oct. 2018.

III.3.3. Birds of a Feather

1. "Latest MPICH works at BSC (To be BSC-MPI)", in *MPICH: A High-Performance Open--Source MPI Implementation. The International Conference for High Performance Computing, Networking, Storage and Analysis (SC19)*, Denver, CO, USA. Nov. 2019.
2. "A novel tool for analysing benefits of data placement in multi-level memory hierarchies", in *Multi-Level Memory and Storage for HPC, Data Analytics & AI. ISC High Performance*, Frankfurt, Germany, June 2019.

III.3.4. Invited Talks in Institutions

1. "Supercomputación: qué es, para qué sirve y cómo la avanzamos desde la investigación en el BSC-CNS". Universidade da Coruña, Coruña, Spain. 1 hour, Apr. 2019.
2. "Programming models and heterogeneity in HPC". Foundation for Research and Technology - Hellas (FORTH), Heraklion, Greece, Nov. 2017.
3. "Virtualization of accelerators in high performance clusters". Argonne National Laboratory, Argonne, IL, USA, Oct. 2012.

III.3.5. Invited Talks in Conferences, Workshops, and Symposia

1. A. J. Peña. "EPEEC: Europe toward high coding productivity for Exascale", in *27th International European Conference on Parallel and Distributed Computing (Euro-Par)*, Online, Sep. 2021.
2. A. J. Peña. "HPC & resource heterogeneity", in *Convergence of Big-Data Analytics, Cloud, and High-performance Computing with EVOLVE, HiPEAC Computer Systems Week Autumn 2019*, Bilbao, Spain, Oct. 2019.
3. A. J. Peña. "The H2020 EPEEC Vision to Programming Productivity at Exascale", in *A Structured Approach for Programming Extreme Scale and Heterogeneous Systems* Workshop, Zurich, Switzerland, Sep. 2019.

4. A. J. Peña. “EPEEC: Productivity at Exascale”, in *Workshop on Platform-driven e-infrastructure innovations*, Amsterdam, The Netherlands, Oct. 2018.
5. A. J. Peña. “Best GPU code practices combining OpenACC, CUDA, and OmpSs”, in *Workshop on Open Source Supercomputing (OpenSuCo)*, Frankfurt, Germany, June 2017.
6. **A. J. Peña** and R. Mayo, “rCUDA 4: GPGPU as a service in HPC clusters”, in *HPC Advisory Council Spain Conference*, Málaga, Spain, Sep. 2012.
7. F. Silla and **A. J. Peña**. “rCUDA, an approach to provide remote access to GPU computational power”, in *HPC Advisory Council Switzerland Conference*, Lugano, Switzerland, Mar. 2012.

III.3.6. Invited Talks in Exhibition Booths

1. "EPEEC: European joint Effort toward a Highly Productive Programming Environment for Heterogeneous Exascale Computing", in PRACE Booth at ISC 2021 Digital, June 2021.
2. A. J. Peña, “Breaking the DRAM size wall for DNN inference and homomorphic encryption”, in Intel Vendor Use-Case, *ISC High Performance*, Virtual, June 2021.
3. A. J. Peña, “A tool for best use of 3D XPoint technology for HPC and AI compelling workloads”, in Intel Booth, *ISC High Performance*, Frankfurt, Germany, June 2019.

III.4 Other Dissemination Activities

1. P. Balaji, T. Hoefler, A. J. Peña, and Y. Guo. “Advanced MPI Programming”, in *ISC High Performance*, Virtual, June 2021 (8h).
2. A. J. Peña, M. Jordà, S. Garcia de Gonzalo, O. Korakitis, and K. Matsumura. “Introduction to OpenACC”. PRACE Advanced Training Centre, Barcelona Supercomputing Center, Barcelona, Spain. 1 day, Apr. 2021.
3. A. J. Peña, M. Jordà, S. Garcia de Gonzalo, S. Rai. “Introduction to CUDA programming”. PRACE Advanced Training Centre, Barcelona Supercomputing Center, Barcelona, Spain. 4 days, Apr. 2021.
4. A. J. Peña, P. Radojkovic, and M. Jordà. “Introduction to Heterogeneous Memory Usage”. PRACE Advanced Training Centre, Barcelona Supercomputing Center, Barcelona, Spain. 1 day, Feb. 2021.
5. A. J. Peña, P. Radojkovic, and M. Jordà. “Introduction to Heterogeneous Memory Usage”. PRACE Advanced Training Centre, Barcelona Supercomputing Center, Barcelona, Spain. 1 day, Feb. 2020.
6. A. J. Peña, L. Toledo, and M. Jordà. “Use and exploitation of GPU cards for scientific computing”. Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas (CIEMAT). Madrid, Spain. 4 days. Jan. 2020.
7. A. J. Peña. “Enabling energy-efficient computing for exascale with EPEEC”, in HiPEACinfo, vol. 59, pp. 31. Jan. 2020.
8. A. J. Peña. “The EPEEC H2020 Project: Programming productivity at exascale”, in PRACE Booth at the International Conference for High Performance Computing, Networking, Storage and Analysis (SC19), USA. Nov. 2019.
9. P. Balaji, T. Hoefler, A. J. Peña, and Yanfei Guo. “Advanced MPI”, in *ISC High Performance*, Frankfurt, Germany, June 2019 (8h).
10. A. J. Peña. “MPI-3, new features and differences with previous MPI standards. Advanced MPI techniques and hands-on sessions”. Centre Informatique National de l'Enseignement Supérieur (CINES), Montpellier, France. 8 hours. June 2019.
11. A. J. Peña, M. Jordà, L. Toledo, and O. Korakitis. “Introduction to CUDA programming”. PRACE Advanced Training Centre, Barcelona Supercomputing Center, Barcelona, Spain. 4 days, Apr. 2019.
12. A. J. Peña. “Introduction to OpenACC”. PRACE Advanced Training Centre, Barcelona Supercomputing Center, Barcelona, Spain. 2 days, Apr. 2019.
13. A. J. Peña. “Introduction to Heterogeneous Memory Usage”. PRACE Advanced Training Centre, Barcelona Supercomputing Center, Barcelona, Spain. 1 day, Feb. 2019.
14. P. Balaji and A. J. Peña. “The SC Technical Program: A Powerful Research Engine & Rich Collection of Opportunities”, in SC19 Blog, Feb. 2019.

15. A. J. Peña. "Multi-GPU Programming and CUDA Interoperability (MPI, OpenACC)". Programming and tUning Massively Parallel Systems + Artificial Intelligence (PUMPS+AI) Summer School. Barcelona, Spain. 1.5 hours, July 2018.
16. T. Hoefler and A. J. Peña. "Advanced MPI", in *ISC High Performance*, Frankfurt, Germany, June 2018 (8h).
17. A. J. Peña. "Programming NVIDIA GPUs with CUDA". Universitat Politècnica de Catalunya (UPC). Association for Computing Machinery (ACM), Barcelona, Spain. 2 hours, May 2018.
18. A. J. Peña. "Introduction to OpenACC". Graphics Cards and Accelerators. Universitat Politècnica de Catalunya (UPC), Barcelona, Spain. 2 hours, May 2018.
19. P. Farre, G. Ozen, and A. J. Peña. "Best GPU code practices combining OpenACC, CUDA, and OmpSs", in *GPU Technology Conference (GTC)*, Silicon Valley, USA, Mar. 2018 (2h).
20. X. Martorell, X. Teruel, and A. J. Peña, "Parallel programming with MPI and OpenMP". Universidad Autónoma de Madrid, Spain. 2 days, Nov. 2017.
21. "Parallel Programming Workshop". PRACE Advanced Training Centre, Barcelona Supercomputing Center, Barcelona, Spain. 2 days, Oct. 2017.
22. P. Farre and A. J. Peña. "Best GPU code practices combining OpenACC, CUDA, and OmpSs", in *GPU Technology Conference Europe (GTC Europe)*, Munich, Germany, Oct. 2017 (1.5h).
23. A. J. Peña and M. Hidayetoglu. "Multi-GPU Programming and CUDA Interoperability (MPI, OpenACC)". Programming and tUning Massively Parallel Systems (PUMPS) Summer School, Barcelona, Spain. 1.5 hours, June 2017.
24. P. Farre, G. Ozen, and A. J. Peña. "Best GPU code practices combining OpenACC, CUDA, and OmpSs", in *GPU Technology Conference (GTC)*, Silicon Valley, USA, May 2017 (2h).
25. A. J. Peña and P. Valero. "Introduction to OpenACC". PRACE Advanced Training Centre, Barcelona Supercomputing Center, Barcelona, Spain. 2 days, Apr. 2017.
26. A. J. Peña. "GPU programming models and their combinations". Universidad de Córdoba, Spain. 4 hours, Apr. 2017.
27. X. Martorell, X. Teruel, and A. J. Peña, "Parallel programming with MPI and OpenMP". Universidad Autónoma de Madrid, Spain. 2 days, Nov. 2016.
28. "Parallel Programming Workshop". PRACE Advanced Training Centre, Barcelona Supercomputing Center, Barcelona, Spain. 2 days, Oct. 2016.
29. A. J. Peña. "Introduction to CUDA programming". PRACE Advanced Training Centre, Barcelona Supercomputing Center, Barcelona, Spain. 4 days, July 2016.
30. P. Balaji, R. Thakur, K. Raffenetti, A. J. Peña, and M. Si. "Advanced parallel programming with MPI-3". Argonne National Laboratory, Argonne, IL, USA. 0.5 days, June 2015.
31. P. Balaji, R. Thakur, K. Raffenetti, A. J. Peña, and M. Si. "Introduction to MPI". Argonne National Laboratory, Argonne, IL, USA. 0.5 days, June 2015.
32. A. J. Peña. "Web-based remote telescope control". Astronomical Observatory, Universitat de València, Valencia, Spain. 1 hour, Mar. 2009.
33. A. J. Peña. "Astroadapt: Free software for persons suffering mobile disability". Astronomical Observatory, Universitat de València, Valencia, Spain. 1 hour, Feb. 2009.

III.5 Communication Activities

1. AI Business. Intel and Barcelona Supercomputing Center succeed in encrypting large neural networks. Sep. 2021. https://aibusiness.com/document.asp?doc_id=771912
2. Today.in-24. BSC-CNS runs neural networks encrypted with Intel Xeon CPUs and Optane memory for the first time. Sep. 2021. https://today.in-24.com/News/326233.html
3. datanami. Barcelona Supercomputing Center Powers Encrypted Neural Networks with Intel Tech. Sep. 2021. https://www.datanami.com/2021/09/03/barcelona-supercomputing-center-powers-encrypted-neural-networks-with-intel-tech/

4. The Next Platform. Boosting memory capacity and performance while saving megawatts. Dec. 2020. https://www.nextplatform.com/2020/12/08/boosting-memory-capacity-and-performance-while-saving-megawatts/
5. Podcast. Antonio Peña from EPEEC (on exascale computing). July 2020. https://soundcloud.com/user-591729646/bpss-006-antonio-pena-from-epeec-on-exascale-computing?in=user-591729646/sets/big-problems-small-solutions
6. The Next Platform. Building an ecosystem for heterogeneous memory supercomputing. July 2020. https://www.nextplatform.com/2020/07/27/building-an-ecosystem-for-heterogeneous-memory-supercomputing/
7. HPCwire. BSC research accelerates HPC workloads with less power-hungry DRAM. July 2020. https://www.hpcwire.com/off-the-wire/bsc-research-accelerates-hpc-workloads-with-less-power-hungry-dram/
8. Intel Customer Spotlight. Intelligent allocation of data to Intel® Optane™ persistent memory stores more data close to CPU with fewer DIMMs. July 2020. https://www.intel.com/content/www/us/en/customer-spotlight/stories/barcelona-supercomputing-center-customer-story.html
9. Interview by Robert Roe. EPEEC European programming. Scientific Computing World, no. 171, pp. 4-5, Spring 2020. https://content.yudu.com/web/tzly/0A43wlf/SCWSpri2020/html/index.html. ISSN 1744-8026. Also in insideHPC: https://insidehpc.com/2020/04/epeec-project-fosters-heterogeneous-hpc-programming-in-europe.
10. Booth Staff, Barcelona Supercomputing Center (BSC). *The International Conference for High Performance Computing, Networking, Storage and Analysis (SC19)*. Denver, CO, USA, Nov. 2019.
11. A. J. Peña. "Supercomputadors i la seva programació per a la recerca científica". European Researchers' Night. Barcelona, Spain. Sep. 2019.
12. Booth Staff, Barcelona Supercomputing Center (BSC). *ISC High Performance*, Frankfurt, Germany, June 2019.
13. Booth Staff, Barcelona Supercomputing Center (BSC). *The International Conference for High Performance Computing, Networking, Storage and Analysis (SC18)*. Dallas, TX, USA, Nov. 2018.
14. A. J. Peña. "Supercomputació: què és, per a què serveix i com l'avancem des de la recerca en Barcelona". European Researchers' Night. Barcelona, Spain. Sep. 2018.
15. A. J. Peña. "Marie Sklodowska-Curie Individual Fellowships. Info & Best Practices". *Programming and tUning Massively Parallel Systems + Artificial Intelligence (PUMPS+AI)* Summer School. Barcelona, Spain. July 2018.
16. Booth Staff, Barcelona Supercomputing Center (BSC). *ISC High Performance*, Frankfurt, Germany, June 2018.
17. A. J. Peña. "Marie Sklodowska-Curie Individual Fellowships. Info & Best Practices". *5th BSC Severo Ochoa Doctoral Symposium*, Barcelona Supercomputing Center, Spain. 0.5 hours, Apr. 2018.
18. Booth Staff, Barcelona Supercomputing Center (BSC). *The International Conference for High Performance Computing, Networking, Storage and Analysis (SC17)*. Denver, CO, USA, Nov. 2017.
19. A. J. Peña. "Marie Curie Individual Fellowships". *Programming and tUning Massively Parallel Systems (PUMPS)* Summer School. Barcelona, Spain. June 2017.
20. Booth Staff, Barcelona Supercomputing Center (BSC). *ISC High Performance*, Frankfurt, Germany, June 2017.
21. Booth Staff, Barcelona Supercomputing Center (BSC). *ISC High Performance*, Frankfurt, Germany, June 2016.

III.6 Organization of Research and Dissemination Activities

III.6.1 Steering Committee Member for International Conferences and Workshops

1. Organizing Member, IEEE International Conference on Cluster Computing (Cluster). 2021 – 2025.
2. General Member, IEEE International Conference on Cluster Computing (Cluster). 2021 – 2023.

3. The International Workshop on Accelerators and Hybrid Exascale Systems (AsHES). Since 2020.

III.6.2 Chair Roles for International Conferences and Workshops

1. General Co-chair. IEEE International Conference on Cluster Computing (IEEE Cluster). Santa Fe, NM, USA, Sep. 2023.
2. Birds of a Feather (BoF) Chair. The International Conference for High Performance Computing, Networking, Storage and Analysis (SC22). USA, Nov 2022.
3. Communications Liaison for Technical Program. The International Conference for High Performance Computing, Networking, Storage and Analysis (SC21). St. Louis, MO, USA, Nov 2021
4. Virtual Arrangements Co-chair. IEEE International Conference on Cluster Computing (IEEE Cluster). Portland, OR, USA, Sep. 2021.
5. More than HPC Plenary Co-chair. The International Conference for High Performance Computing, Networking, Storage and Analysis (SC20). Atlanta, GA, USA, Nov. 2020.
6. Program Co-chair. 27th European MPI Users' Group Meeting (EuroMPI/USA). Austin, TX, USA, Sep. 2020.
7. General Co-chair. 1st Workshop on Heterogeneous Memory Systems (HMEM). Barcelona, Spain, June 2020.
8. Session Lead. 15th Workshop on Virtualization in High-Performance Cloud Computing (VHPC). Frankfurt, Germany, June 2020.
9. Technical Program Vice-chair. The International Conference for High Performance Computing, Networking, Storage and Analysis (SC19). Denver, CO, USA, Nov. 2019.
10. Track Chair (Programming Models). The 31st International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD). Campo Grande, Brazil, Oct. 2019.
11. Discussion Lead. "Programming Models for Heterogeneous Systems" and "Data Placement and Movement on Heterogeneous Memories". A Structured Approach for Programming Extreme Scale and Heterogeneous Systems Workshop, Zurich, Switzerland, Sep. 2019.
12. General Chair. The Ninth International Workshop on Accelerators and Hybrid Exascale Systems (AsHES). Rio de Janeiro, Brazil, May 2019.
13. General Chair. 25th European MPI Users' Group Meeting (EuroMPI). Barcelona, Spain, Sep. 2018.
14. Program Co-chair. The Eight International Workshop on Accelerators and Hybrid Exascale Systems (AsHES). Vancouver, Canada, May 2018.
15. Session Chair (GPUs and Communication). The International Conference for High Performance Computing, Networking, Storage and Analysis (SC17). Denver, CO, USA, Nov. 2017.
16. Proceedings Chair. 24th European MPI Users' Group Meeting (EuroMPI/USA). Chicago, IL, USA, Sep. 2017.
17. Session Chair (Memory and Topology). 24th European MPI Users' Group Meeting (EuroMPI/USA). Chicago, IL, USA, Sep. 2017.
18. Session Chair (GPU Applications). 46th International Conference on Parallel Processing (ICPP). Bristol, UK, Aug. 2017.
19. Program Co-chair. The Seventh International Workshop on Accelerators and Hybrid Exascale Systems (AsHES). Orlando, FL, USA, May 2017.
20. Program Co-chair. The Sixth International Workshop on Accelerators and Hybrid Exascale Systems (AsHES). Chicago, IL, USA, May 2016.
21. Program Chair. Heterogeneous and Unconventional Cluster Architectures and Applications (HUCAA). Chicago, IL, USA, Sep. 2015.
22. Web Co-chair. IEEE International Conference on Cluster Computing (Cluster). Chicago, IL, USA, Sep. 2015.
23. Session Chair (Data Movement and I/O). The Seventh International Workshop on Parallel Programming Models and Systems Software for High-End Computing (P2S2). Minneapolis, MN, USA, Sep. 2014.

24. Publicity Co-chair. The Fourth International Workshop on Accelerators and Hybrid Exascale Systems (AsHES). Phoenix, AZ, USA, May 2014.
25. Volunteer Student at the Local Organization Committee. III Computer Science Spanish Conference (CEDI). Valencia, Spain, Sep. 2010.

III.6.3 Organization of Courses and Other Technical Events

1. Local Organization Chair. 9th-11th Programming and tUning Massively Parallel Systems + Artificial Intelligence (PUMPS+AI) Summer School. Barcelona, Spain, July 2018, June 2019, July 2021.
2. Organizer. 1st-5th "Introduction to OpenACC". PRACE Advanced Training Centre, Barcelona Supercomputing Center, Barcelona, Spain, July 2016, Apr. 2017, Apr. 2018, Apr. 2019, Apr. 2021.
3. Organizer. 5 editions. "Introduction to CUDA Programming". PRACE Advanced Training Centre, Barcelona Supercomputing Center, Barcelona, Spain, July 2016, Apr. 2017, Apr. 2018, Apr. 2019, Apr. 2021.
4. Organizer. 1st-3rd "Introduction to Heterogeneous Memory Usage". PRACE Advanced Training Centre, Barcelona Supercomputing Center, Barcelona, Spain. 1 day, Feb. 2019, Feb. 2020, Feb. 2021
5. General Co-chair. 1st-2nd MareNostrum Hackathon (MNHACK). Barcelona, Spain, Oct. 2018, Nov. 2019.
6. Co-Organizer. Thematic Session on Programming Models for Upcoming Supercomputers. HiPEAC Computer Systems Week (CSW). Bilbao, Spain, Oct. 2019.
7. Co-organizer. 1st-3rd Annual BSC/UPC HPC Hackathon. Barcelona, Spain, Oct. 2016, Nov. 2017, Nov. 2018.
8. Local Organization Chair. 7th-8th Programming and tUning Massively Parallel Systems (PUMPS) Summer School. Barcelona, Spain, July 2016, June 2017.
9. Organizer. Basic Programming of Multicore and Many-Core Processors for Image and Video Processing. Barcelona Supercomputing Center, Barcelona, Spain, June 2017.
10. Co-chair. IEEE International Scalable Computing Challenge (SCALE). Madrid, Spain, May 2017.
11. Co-organizer. Enhancing Software Development for Emerging Platforms Using Algorithms and Performance Tools. SIAM CSE Minisymposium. Salt Lake City, UT, USA, Mar. 2015.

III.7 Technical Committees

III.7.1 Advisory Boards

1. oneAPI Technical Advisory Board Member. Intel. Since Nov. 2019.
2. Scientific Advisory Board Member. Exascale Programming Models for Heterogeneous Systems (EPiGRAM-HS) H2020 EC Project. Sep. 2018 – Aug. 2021.

III.7.2 Project Proposal Reviews

1. Austrian Science Fund (FWF), Austria. 2019.

III.7.3 Award Selection Committees

1. ACM SIGHPC Computational & Data Science Fellowships 2021.
2. Best Poster and Hackathon Awards Committee. Programming and Tuning Massively Parallel Systems + Artificial Intelligence Summer School (PUMPS+AI). Barcelona, Spain, June 2019.
3. IEEE TCHPC Award for Excellence for Early Career Researchers in High Performance Computing. Dallas, TX, USA. Nov. 2018.
4. Best Poster and Hackathon Awards Committee. Programming and Tuning Massively Parallel Systems + Artificial Intelligence Summer School (PUMPS+AI). Barcelona, Spain, July 2018.
5. Best Poster, Clinic, and Achievement Awards Committee. Programming and Tuning Massively Parallel Systems Summer School (PUMPS). Barcelona, Spain, June 2017.

6. Best Poster and Clinic Awards Committee. Programming and Tuning Massively Parallel Systems Summer School (PUMPS). Barcelona, Spain, July 2016.
7. Best Technical Paper. IEEE Cluster. Indianapolis, IN, USA, Sep. 2013.

III.7.4 Program Committee for International Conferences and Workshops

1. 36th International Parallel and Distributed Processing Symposium (IPDPS). Lyon, France. May 2022.
2. International Conference on High Performance Computing in Asia-Pacific Region (HPC Asia). Kobe, Japan. Jan. 2022.
3. 11th International Workshop on Runtime and Operating Systems for Supercomputers (ROSS 2021). St. Louis, Missouri. Nov. 2021.
4. Sixth Int'l Workshop on Extreme-Scale Programming Models and Middleware (ESPM2). St. Louis, Missouri. Nov. 2021.
5. 50th International Conference on Parallel Processing (ICPP). Chicago, IL, USA. Aug. 2021.
6. Sixth International Workshop on Communication Architectures for HPC, Big Data, Deep Learning and Clouds at Extreme Scale (ExaComm). Frankfurt, Germany. June 2021.
7. 35th International Parallel and Distributed Processing Symposium (IPDPS). Portland, Oregon, USA. May 2021.
8. IEEE International Conference on Cluster Computing (Cluster). Kobe, Japan. Sep. 2020.
9. The 32nd International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD). Porto, Portugal, Sep. 2020.
10. 26th International European Conference on Parallel and Distributed Computing (Euro-Par). Warsaw, Poland. Aug. 2020.
11. 34th International Parallel and Distributed Processing Symposium (IPDPS). New Orleans, LA, USA. May 2020. Primary Committee Member.
12. IEEE/ACM International Symposium on Cluster, Cloud, and Grid Computing (CCGrid). Melbourne, Australia. May 2020
13. SupercomputingAsia (SCA20). Singapore. Feb. 2020.
14. IEEE International Conference on Cluster Computing (Cluster). Albuquerque, NM, USA. Sep. 2019.
15. 26th European MPI Users' Group Meeting (EuroMPI). Zurich, Switzerland. Sep. 2019.
16. 25th International European Conference on Parallel and Distributed Computing (Euro-Par). Göttingen, Germany, Aug. 2019.
17. The 5th IEEE International Conference on Data Science and Systems (DSS). China, Aug. 2019.
18. 48th International Conference on Parallel Processing (ICPP). Kyoto, Japan. Aug. 2019.
19. 9th International Workshop on Runtime and Operating Systems for Supercomputers (ROSS). Phoenix, AZ, USA, June 2019.
20. 33rd International Parallel and Distributed Processing Symposium (IPDPS). Rio de Janeiro, Brazil. May 2019. Primary Committee Member.
21. 12th IEEE International Scalable Computing Challenge (SCALE). Larnaca, Cyprus, May 2019.
22. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS). Madison, WI, USA. Mar. 2019.
23. SupercomputingAsia (SCA19). Singapore, Mar. 2019.
24. The International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD). Lyon, France. Sep. 2018.
25. IEEE International Conference on Cluster Computing (Cluster). Belfast, UK. Sep. 2018.
26. 3rd International Workshop on Performance Portable Programming Models for Accelerators (P^3MA). Frankfurt, Germany. June 2018.
27. Fourth International Workshop on Communication Architectures for HPC, Big Data, Deep Learning and Clouds at Extreme Scale (ExaComm). Frankfurt, Germany. June 2018.

28. 6th Workshop on Runtime and Operating Systems for the Many-core Era (ROME). Vancouver, Canada. May 2018.
29. SupercomputingAsia (SCA18). Singapore, Mar. 2018.
30. The 11th Annual General Purpose computing with Graphics Processing Units (GPGPU-11). Vienna, Austria. Feb. 2018.
31. IEEE International Conference on High Performance Computing and Communications (HPCC). Bangkok, Thailand. Dec. 2017.
32. The International Conference for High Performance Computing, Networking, Storage and Analysis (SC17). Denver, CO, USA. Nov. 2017.
33. Fourth International Workshop on Accelerator Programming Using Directives (WACCPD). Denver, CO, USA. Nov. 2017.
34. The International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD). Campinas, Brazil. Oct. 2017.
35. 24th European MPI Users' Group Meeting (EuroMPI/USA). Chicago, IL, USA. Sep. 2017.
36. IEEE International Conference on Cluster Computing (Cluster). Honolulu, Hawaii, USA. Sep. 2017.
37. 5th Workshop on Runtime and Operating Systems for the Many-core Era (ROME). Santiago de Compostela, Spain. Aug. 2017.
38. The International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms (HeteroPar). Santiago de Compostela, Spain. Aug. 2017.
39. Third International Workshop on Communication Architectures for HPC, Big Data, Deep Learning and Clouds at Extreme Scale (ExaComm). Frankfurt, Germany. June 2017.
40. 31st IEEE International Parallel & Distributed Processing Symposium (IPDPS). Orlando, FL, USA. May 2017. Primary Committee Member.
41. International Conference on High Performance Computing (HiPC). Hyderabad, India. Dec. 2016.
42. The International Conference for High Performance Computing, Networking, Storage and Analysis (SC16). BoF Programming Systems. Salt Lake City, UT, USA. Nov. 2016.
43. Third International Workshop on Accelerator Programming Using Directives (WACCPD). Salt Lake City, UT, USA. Nov. 2016.
44. 4th Workshop on Runtime and Operating Systems for the Many-core Era (ROME). Grenoble, France. Aug. 2016.
45. 16th IEEE International Conference on Scalable Computing and Communications (ScalCom). Toulouse, France. July 2016.
46. The Seventh International Conference on Cloud Computing, GRIDs, and Virtualization (CLOUD COMPUTING). Rome, Italy. Mar. 2016.
47. The 24rd International Conference on Computer Communications and Networks (ICCCN). Las Vegas, NV, USA. Aug. 2015.
48. The Fifth International Workshop on Accelerators and Hybrid Exascale Systems (AsHES). Hyderabad, India. May 2015.
49. The Sixth International Conference on Cloud Computing, GRIDs, and Virtualization (CLOUD COMPUTING). Nice, France. Mar. 2015.
50. International Workshop on Enhancing Parallel Scientific Applications with Accelerated HPC (ESAA). Kyoto, Japan, Sep. 2014.
51. IEEE International Conference on Cluster Computing (Cluster). Madrid, Spain. Sep. 2014.
52. Heterogeneous and Unconventional Cluster Architectures and Applications (HUCAA). Minneapolis, MN, USA. Sep. 2014.
53. The 23rd International Conference on Computer Communications and Networks (ICCCN). Shanghai, China. Aug. 2014.
54. The Fifth International Conference on Cloud Computing, GRIDs, and Virtualization (CLOUD COMPUTING). Venice, Italy. May 2014.

55. The Fourth International Workshop on Accelerators and Hybrid Exascale Systems (AsHES). Phoenix, AZ, USA. May 2014.
56. 5th IEEE International Conference on Cloud Computing Technology and Science (CloudCom). Bristol, UK. Dec. 2013.

III.7.5 Editorial Boards for International Journals

1. Guest Editor. Applied Sciences, Special Issue: State-of-the-Art High-Performance Computing and Networking, MDPI. 2021. SJR Q2 (SJR 2020).
2. Topic Editor / Topical Advisory Panel Member. Applied Sciences, MDPI. Jan. 2021 – Jan. 2023. SJR Q2 (SJR 2020).
3. Co-editor. Special Section on Parallel and Distributed Computing Techniques for AI, ML, and DL. IEEE Transactions on Parallel and Distributed Systems. 2021. SJR Q1 (SJR 2020).
4. Managing Guest Editor. International Journal on Parallel Computing, Special Issue on Applications and System Software for Hybrid Exascale Systems, Elsevier. Vol. 91, Jan. 2020. SJR Q3.
5. Managing Guest Editor. International Journal on Parallel Computing, Special Issue on Applications for the Heterogeneous Computing Era, Elsevier. Vol. 77, Sep. 2018. SJR Q2.
6. Academic Editor. Scientific Programming, Hindawi. Since July 2018. SJR Q3.
7. Managing Guest Editor. International Journal on Parallel Computing, Special Issue on Applications for the Heterogeneous Computing Era, Elsevier. Vol. 68, Oct. 2017. SJR Q2.

III.7.6 Reviewer for International Journals

1. Access, IEEE, SJR Q1. 1 review since 2020.
2. Transactions on Computers (TC), IEEE, SJR Q1. 2 reviews since 2019.
3. Transactions on Industrial Informatics, IEEE. SJR Q1. 1 review since 2019.
4. Transactions on Architecture and Code Optimization (TACO), ACM. SJR Q3. 3 reviews since 2017.
5. International Journal of Parallel Programming (IJPP), Springer. SJC Q3. 1 review since 2016.
6. Trans. on Circuits and Systems for Video Technology (TCSVT), IEEE. SJR Q1. 1 review since 2016
7. Big Data Research (BDR), Elsevier. SJR Q1. 1 review since 2016.
8. Micro, IEEE. SJR Q1. 1 review since 2016.
9. Journal of Parallel and Distributed Computing (JPDC), Elsevier. SJR Q2. 12 reviews since 2016.
10. Int. J. of High Perf. Computing Applications (IJHPCA), SAGE. SJR Q2. 7 reviews since 2015.
11. INFOCOMP Journal of Computer Science. 1 review since 2015.
12. Simulation Modelling Practice and Theory (SIMPAT), Elsevier. SJR Q1. 1 review since 2015.
13. Parallel Processing Letters (PPL), World Scientific. SJR Q3. 3 reviews since 2013.
14. Transactions on Cloud Computing (TCC), IEEE Computer Society. SJR Q1. 11 reviews since 2013.
15. Trans. on Parallel and Distributed Systems (TPDS), IEEE. SJR Q1. 9 reviews since 2013.
16. Parallel Computing Journal (PARCO), Elsevier. SJR Q2. 7 reviews since 2013.
17. Journal of Automated Software Engineering (JASE), Springer. SJR Q1. 1 review since 2012.
18. Future Generation Computer Systems (FGCS), Elsevier. SJR Q1. 7 reviews since 2012.
19. Concurrency & Computation: Practice & Experience (CCPE), Wiley. SJR Q2. 4 reviews since 2010.

III.7.7 Additional Reviewer for International Conferences and Workshops

1. *The International Conference for High Performance Computing, Networking, Storage and Analysis (SC16).* Salt Lake City, UT, USA, Nov. 2016.
2. *The 24th International Conference on Parallel Architectures and Compilation Techniques (PACT).* San Francisco, CA, USA, Oct. 2015.
3. *IEEE Hot Interconnects (HOTI).* Santa Clara, CA, USA, Aug. 2015.

4. *IEEE International Conference on High Performance Computing (HiPC)*. Goa, India, Dec. 2014.
5. *The International Conference for High Performance Computing, Networking, Storage and Analysis (SC14)*. New Orleans, LA, USA, Nov. 2014.
6. *International European Conference on Parallel and Distributed Computing (Euro-Par)*. Aachen, Germany, Aug. 2013.
7. *International Supercomputing Conference (ISC)*. Leipzig, Germany, June 2013.
8. *The 13th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGrid)* – Doctoral Symposium. Delft, The Netherlands, May 2013.
9. *3rd Intl. Workshop on Accelerators and Hybrid Exascale Systems (AsHES)*. Boston, USA, May 2013.
10. *22nd International Heterogeneity in Computing Workshop (HCW)*. Boston, MA, USA, May 2013.
11. *Intl. Workshop on Heterogeneous Architectures and Computing (HAC)*. Leganes, Spain, July 2012.
12. *The 14th International Conference on HPC & Communications (HPCC)*. Liverpool, UK, June 2012.
13. *8th Intl. Conf. on Parallel Processing & Applied Mathematics (PPAM)*. Wroclaw, Poland, Sep. 2009.

III.8 Involvement in Standardization and Policy Making Efforts

1. Strategic Research Agenda 4 (SRA 4), European Technology Platform for High Performance Computing (ETP4HPC). Mar. 2020. https://www.etp4hpc.eu/sra4-contributors.html
2. MPI: A Message-Passing Standard, Version 3.1. Message Passing Interface Forum. Releas. June 2015.
3. OpenFabrics Interfaces (OFI) v1.0. Released May 2015.

III.9 Professional Memberships

1. Sr. Member of IEEE since July 2021. IEEE Member since 2013. IEEE TCSC Member since 2014. IEEE Comp. Soc. since 2016.
2. Sr. Member of ACM since Apr. 2021. Member since 2014.
3. Member of Marie Curie Alumni Association since Mar. 2021.
4. Full member of HiPEAC since Mar. 2017.

III.10 Other Activities

1. Hackathon Mentor. Programming and tUning Massively Parallel Systems + Artificial Intelligence (PUMPS+AI) Summer School. Barcelona, Spain, July 2018.
2. Member of the BSC Outreach Working Group. Since May 2016.
3. Moderator of the hpc-announce@mcs.anl.gov mailing list from May 2013 to July 2015.

IV. PROFESSIONAL TRAINING AND ADDITIONAL EDUCATION

IV.1 Internships

Type: Graduate
Center: Swiss National Supercomputing Centre (CSCS), Swiss Federal Institute of Technology (ETH) Zürich
Main Responsibilities: Development of a port for the NetPIPE communication benchmark for the Cray XE6 network. Extension of NetPIPE to characterize accelerator-accelerator communication over HPC interconnects. Early port of LAMMPS to rCUDA. Benchmarking and evaluation of accelerator-based HPC systems. Performance characterization of GPUDirect-RDMA on different cluster configurations.
Dates: Sep. 2011 – Dec. 2011 and Oct. 2012 **Supervisor:** Dr. Sadaf Alam

Type: Undergraduate
Organization: Innova Advanced Consulting (Spain)
Main Responsibilities: Analysis and programming tasks on *Microsoft Business Solutions – Navision.* Eventual consulting and teaching activities.
Dates: July 2005 – May 2006

IV.2 Other Fellowships

Department: Basic and Clinical Psychology and Psychobiology, Universitat Jaume I (Spain).
Main Activities and Responsibilities: Changes on the methodology of using The Internet as a self-learning tool. Designed and developed an online practical session.
Dates: Feb. 2004 – July 2004.
Position: Collaboration Fellowship.

IV.3 Languages

1. Native Spanish.
2. English. CEFR C2 (Mastery or Proficiency). Official Languages School of Castelló (Spain). Sep 2017.
3. Valencian. CEFR C2 (Mastery or Proficiency). Junta Qualificadora de Coneixements del Valencià, Conselleria de Cultura, Educació i Esport, Generalitat Valenciana. July 2005.

IV.4 Additional Education

IV.4.1 Training for Team Leading, Management, and Professional Development

1. Working remotely: Managing fatigue and maintaining balance. 2h. BSC, June 2021.
2. Fundamentals of successful remote meetings. 6h. Barcelona Supercomputing Center, June 2021.
3. The science of wellbeing and stress management. 6h. Barcelona Supercomputing Center, June 2021.
4. How to write a competitive ERC StG'20 proposal. 6h. Agència de Gestió d'Ajuts Universitaris i de Recerca (AGAUR), Generalitat de Catalunya, Barcelona, Spain, July 2019.
5. How to Conduct Effective Meetings. 4h. Barcelona Supercomputing Center, Spain, June 2018.
6. Developing High Performance Teams. 4h. Barcelona Supercomputing Center, Spain, May 2018.
7. Impact Public Speaking. 4h. Barcelona Supercomputing Center, Barcelona, Spain, May 2018.
8. How to be an Effective Facilitator. 4h. Barcelona Supercomputing Center, Spain, Nov. 2017.
9. Goal Setting & Staff Performance Review. 4h. Barcelona Supercomputing Center, Spain, Nov. 2017.
10. Neurolinguistics Programming & Emotional Intelligence in Conflict-Solving. 4h. BSC, Jul. 2017.
11. Colearning. 4h. Barcelona Supercomputing Center, Barcelona, Spain, Oct. 2016.
12. People and Team Direction. 8h. Barcelona Supercomputing Center, Barcelona, Spain, July 2016.
13. Project Management for non Project Managers. 6h. Barcelona Supercomputing Center, June 2016.
14. How to Write the Impact of a H2020 Proposal. 3.5h. Barcelona Supercomputing Center, Feb. 2016.
15. Addressing Impact in Horizon 2020 Proposals. 4h. Barcelona Supercomputing Center, Nov. 2015.

IV.4.2 Specific Education for Research on High Performance Computing

1. Programming and Tuning Massively Parallel Systems (PUMPS). Advanced Track. Barcelona, Spain, July 2010.
2. Sixth International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES). Terrassa, Spain, July 2010.
3. Fifth International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES). Terrassa, Spain, July 2009.

IV.4.3 Higher Education Courses

1. Mobile Devices Programming. Postgraduate Studies and Continuous Education Center, Universitat Jaume I, Spain, Feb. 2006 – May 2006.
2. Voice over IP. Postgraduate Studies and Continuous Education Center, Universitat Jaume I, Spain, Apr. 2006.
3. Computer Vision and Applications. Postgraduate Studies and Continuous Education Center, Universitat Jaume I, Spain, Mar. 2005.