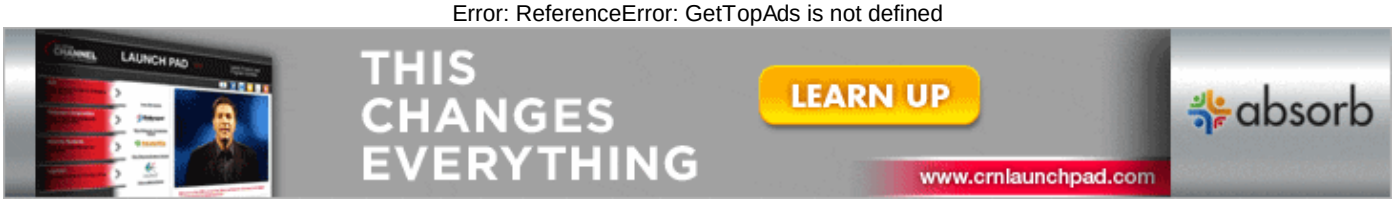

Intel's 'Knight's Corner' Processor Hits Speed Of One Teraflop

By Kristin Bent, CRN 6:06 PM EST mié. nov. 16, 2011

Intel took a step closer toward exascale computing on Wednesday after its new "Knight's Corner" co-processor delivered more than one teraflop of double precision floating point performance during a demonstration at the SC11 event.

When released, the 22-nm "Knight's Corner" will be the first commercial processor to leverage Intel's Many Integrated Core (MIC) architecture, designed to process highly parallel workloads, while offering compatibility with existing x86 programming model and tools. The benefits of MIC architecture for tasks including weather modeling, tomography, proteins folding and advanced materials simulation were demonstrated at the event.

While Intel didn't disclose the co-processor's formal release date or exact specs, it did say that the new chip will feature "more than" 50 cores.

Rajeeb Hazra, general manager of technical computing at the Intel datacenter and connected systems group, stressed the significance of a single chip breaking the one teraflop barrier.

"Intel first demonstrated a Teraflop supercomputer utilizing 9,680 Intel Pentium Pro processors in 1997 as part of Sandia Lab's 'ASCI RED' system," Hazra said in a statement. "Having this performance now in a single chip based on Intel MIC architecture is a milestone that will once again be etched into HPC history."

Despite its magnitude, "Knight's Corner" is only a small step within Intel's overall journey toward exascale computing.

According to the chipmaker, its goal is to deliver exascale-level performance by 2018, meaning the delivery of a technology that would enable a supercomputer to run 100 times faster than the max level of performance available today. Hazra shed some light on how the firm plans to achieve such an aggressive goal.

Working closely with the HPC community, he noted at the event, is top of mind.

In an effort to do just that, Intel has partnered with the Barcelona Supercomputing Center (BSC) to create the Exascale Laboratory in Barcelona, Intel's fourth European Exascale R&D lab. The focus of this lab, specifically, will be scalability within the programming and runtime systems of exascale machines.

Intel and the Science and Technology Facilities Council (STFC) have also announced a collaboration to develop and test technology for future supercomputing platforms.