Detailed agenda:

**Feb. 12th, 2019 - Day 1**

10:00h Welcome (BSC/Xilinx)

10:05h
1. Introduction of Vivado HLS (Xilinx)
2. Introduction of OmpSs@FPGA (BSC/UPC)
3. Environment explanation of OmpSs@FPGA (BSC/UPC)

   - Generate to HLS a Matrix Multiply (no optimizations)

11:30h Coffee Break

4-Simulation with HLS (Hands-on Xilinx/OmpSs@FPGA guided)
   Analysis of the HLS project created by the OmpSs@FPGA toolchain

13:30h Lunch

14:00-18:00h
5. Opt. RGB-YUV filter using Vivado HLS and OmpSs@FPGA (Hands-on Xilinx + OmpSs@FPGA team)
   Objective: Analysis and apply optimizations to be able, later on, to execute and obtain a benefit.

   5.1- Timing of naive solution (ARM binary + bitstream) of the code using OmpSs@FPGA (provided with the material)
   5.2- Make a OmpSs@FPGA porting annotating the original code with OmpSs directives
   5.3- Use OmpSs@FPGA toolchain to compile the code up to HLS to obtain the Vivado HLS project
   5.4- Open Vivado HLS to perform the analysis using the Vivado HLS features
   5.5- Add Vivado HLS and analyse their performance impact:
       Directives: tripcount, offload inlining, pipelining, dataflow, fifo depth
   5.6- Use OmpSs@FPGA toolchain to compile from HLS to bitstream and compare execution time to the naive version

**Feb. 13th, 2019 - Day 2**

10:00h Recap first day

10:15h
6. Optimize DCT using OmpSs@FPGA and Vivado HLS directives
Objective: Analysis and optimization

6.1- Timing of naive solution (ARM binary + bitstream) of the code using OmpSs@FPGA (provided with the material)
6.2- Make a OmpSs@FPGA porting annotating the original code with OmpSs directives
6.3- Use OmpSs@FPGA toolchain to compile the code up to HLS to obtain the Vivado HLS project

11:30h Coffee Break

12:00h - 16:00h (Lunch at 13:30h)

6.4- Open Vivado HLS to perform the analysis using the Vivado HLS features
6.5- Add Vivado HLS and analyse their performance impact:
    Directives: pipeline (inner and outer loop), data partition/resource analysis, array partition, dataflow, inline, reshaping
6.6- Use OmpSs@FPGA toolchain to compile from HLS to bitstream and compare execution time to the naive version

16:00h

7-Hardware instrumentation (Internal to the accelerators)

8-Work on user provided applications
    (or propose optimizations for Matrix Multiply)

17:30h Recap of the tutorial

18:00h Adjourn

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