Maspatechnologies, the new BSC spin-off for multicore safety validation for aerospace and automotive domains

The company will develop tools simplifying the generation of evidence on the correctness of the timing behaviour of safety application in critical domains like avionics and automotive.

This technology, called micro-benchmarks, will significantly reduce the cost of end users to provide evidence about the correct timing behaviour of the application on multicore hardware platforms.

BSC has launched a new spin-off, Maspatechnologies, that aims to provide multicore timing analysis solutions in accordance to safety standards for critical embedded systems, including automotive, aerospace and space industry. The main product offered by Maspatechnologies is a software component called microbenchmark technology to be used for timing verification, validations and optimization of software developed for embedded real-time domains. Micro-benchmarks will significantly reduce the cost of end users to provide evidence about the correct timing behaviour of the applications on the target multicore.
The news spin-off will provide multicore support verification and validation tools and services that help critical real-time industries to adopt multicore- manycore- and accelerator-based platforms. In particular, Maspatechnologies tools simplify obtaining evidence for safety application in adherence to safety/certification guidelines in terms of timing. This includes CAST-32A in avionics and ISO 26262 safety standard in automotive.

The company, which will offer both a tool and consultancy services, will be part of the value chain in embedded critical systems, and in particular the software verification and validation activities.

A team of BSC researchers from the Computer Architecture - Operating Systems (CAOS) and CSIC have launched this spin-off.

Jaume Abella and Francisco J. Cazorla, co-founders of the company highlight, that “this is an important step for us to take the technology developed at BSC and CSIC to commercial use, hence returning to the taxpayers their investment in the form of safer transportation systems and highly-qualified jobs”.

**About the technology**

The main invention element is a set of specialized user-level benchmarks that put a configurable, usually high, frequency access load on a target set of processor resources like caches, buses or memory. This so called microbenchmarks, are single-behaviour applications that constantly access the target resources. The invention also includes a set of scripts able to produce microbenchmarks automatically from a description of the target resource. For instance, for a cache the description includes parameters like its associativity, cache line size, and total size. Derived technologies from micro-benchmarks also include software multicore contention models, all with the goal of providing evidence of the correct timing behaviour of applications in multicore-based embedded systems.

Microbenchmarks speed up the adoption of complex hardware in critical real-time systems. By running microbenchmarks against a reference application under analysis, one can get an accurate measure of the impact that resource contention may have on the application’s timing behaviour. Microbenchmarks also comprise a validation loop that works with Performance Monitoring Counters (PMCs) to provide evidence that they achieve their intended goal in stressing different processor resources.

Barcelona Supercomputing Center - Centro Nacional de Supercomputación