Five BSC papers accepted for DAC 2018

The papers cover topics relating to timing analysis, GPU programming, multicores, and mixed criticality, which are becoming increasingly important in key sectors, such as the automotive industry.

This year, five papers by the Computer Architecture – Operating Systems (CAOS) group at BSC have been accepted for presentation at DAC 2018, which will take place in San Francisco on 24-28 June.

The Design Automation Conference (DAC) is the premier symposium for design automation and electronic systems, and the longest-running conference on computer architecture, celebrating its 55th edition this year. Every year, there is significant competition for the best research works to be published at such a prestigious event. DAC is ranked (A+) from the GII-GRIN-SCIE (GGS) Conference Rating and is one amongst a select group of conferences – eight in total – where papers published are eligible for a HiPEAC Paper Award.

Francisco J. Cazorla, leader of the CAOS group at BSC, commented: ‘Having five papers accepted at DAC is a reflection of the outstanding work being carried out by BSC. It is particularly satisfying for me to see that the first authors of three of the five papers are women, showing how BSC’s efforts to combat the gender disparity in this field are paying off.’

The papers cover topics relating to timing analysis, GPU programming, multicores, and mixed criticality, which are becoming increasingly important in key sectors, such as the automotive industry. The full list is as follows:

- ‘Modelling Multicore Contention on the AURIX(TM) TC27x’
BSC authors: Enrique Díaz, Enrico Mezzetti, Leonidas Kosmidis, Jaume Abella, Francisco J. Cazorla
- ‘Measurement-Based Cache Representativeness on Multipath Programs’

BSC authors: Suzana Milutinovic, Jaume Abella, Enrico Mezzetti and Francisco J. Cazorla
- ‘Brook Auto: High-Level Certification-Friendly Programming for GPU-powered Automotive Systems’

BSC/UPC authors: Matina Maria Trompouki, Leonidas Kosmidis
- ‘Cache Side-Channel Attacks and Time-Predictability in High-Performance Critical Real-Time Systems’

BSC authors: David Trilla, Carles Hernandez, Jaume Abella and Francisco J. Cazorla
- Response-Time Analysis of DAG Tasks Supporting Heterogeneous Computing

BSC authors: Maria A. Serrano, Eduardo Quiñones

Further information about the research group can be found on the CAOS webpage.

Find out more about BSC’s efforts to combat the gender gap in computing in the Gender and Diversity Equality Plan.

Barcelona Supercomputing Center - Centro Nacional de Supercomputación