Hybrid BSC RS: RISC-V Near-Memory Processing Accelerators

Objectives

The slides can be downloaded here.

Abstract: The RISC-V architecture has opened new opportunities for many people to innovate in computer design. However to design a chip that can compete in the marketplace against veteran industry computer designers with their vast resources is still a formidable challenge. We propose a solution for specialized accelerators with near-memory processing architectures. We observe the critical technology is the embedded memory because it consumes most of the silicon area and determines the power/bandwidth of the chip. If instead memory is stacked on top of the logic chip, then a much lower cost, less dense, mature technology can be used for the logic. Communication wire power will be lower because the through-silicon via (TSV) interconnect traverses a much smaller distance, offsetting the lower power efficiency of mature logic technology. Design cost of the re-useable hi-tech memory chip is amortized across multiple accelerators. We believe this approach can help smaller organizations with limited resources design commercially competitive novel accelerators.

Short bio: Peter Hsu received his Ph.D. from University of Illinois Urbana-Champaige. He started work at IBM T. J. Watson Research Center on the 801 Project. He joined SGI in 1990 as architect of MIPS R8000 TFP microprocessor; the chip powered fifty TOP500 supercomputers in 1994. Peter co-founded ArtX in 1997 to develop the Nintendo GameCube video game console. He joined Oracle Labs in 2011 as Architect and built a fifty thousand core parallel SQL database accelerator. Peter moved to Europe in 2018 and was visiting professor at EPFL University in Switzerland, then senior researcher at the Barcelona Supercomputing Center. In 2022 he started a consulting company in Spain, Peter Hsu & Associates, S.L.

Speakers

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