

## **Vector Processing-Aware Advanced Clock-Gating Techniques for Low-Power Fused Multiply-Add**

**URL:** <http://ieeexplore.ieee.org/document/8252727/>

**Authors:** [Ratkovi?, Ivan](#) / [Palomar, Oscar](#) / [Stanic, Milan](#) / [Unsal, Osman](#) / [Cristal, Adrian](#) / [Valero, Mateo](#)

**Publication:** IEEE Transactions on Very Large Scale Integration (VLSI) Systems

**Pagination:** 1 - 14

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

---

**Source URL (retrieved on 23 Abr 2024 - 10:47):** <https://www.bsc.es/es/research-and-development/publications/vector-processing-aware-advanced-clock-gating-techniques-low>