

JSRAM: A Circuit-Level Technique for Trading-Off Robustness and Capacity in Cache Memories

URL: <http://ieeexplore.ieee.org/xpl/articleDetails.jsp?reload=true&arnumber=7309554>

Authors: [Ahangari, Hamzeh](#) / [Yalcin, Gulay](#) / [Ozturk, Ozcan](#) / [Unsal, Osman](#) / [Cristal, Adrián](#)

Publication: 2015 IEEE Computer Society Annual Symposium on VLSI

Place Published: Montpellier, France

Pagination: 149-154

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

Source URL (retrieved on 25 Abr 2024 - 05:39): <https://www.bsc.es/es/research-and-development/publications/jsram-circuit-level-technique-trading-robustness-and-capacity>