Mont-Blanc 3: European scalable and power efficient HPC platform

Description

The main target of the Mont-Blanc 3 project "European Scalable and power efficient HPC platform based on low-power embedded technology" is the creation of a new high-end HPC platform (SoC and node) that is able to deliver a new level of performance / energy ratio whilst executing real applications.

The technical objectives are:

1. To design a well-balanced architecture and to deliver the design for an ARM based SoC or SoP (System on Package) capable of providing pre-exascale performance when implemented in the time frame of 2019-2020. The predicted performance target must be measured using real HPC applications.

2. To maximise the benefit for HPC applications with new high-performance ARM processors and throughput-oriented compute accelerators designed to work together within the well-balanced architecture

3. To develop the necessary software ecosystem for the future SoC. This additional objective is important to maximize the impact of the project and make sure that this ARM architecture path will be successful in the market. The project shall build upon the previous Mont-Blanc & Mont-Blanc 2 FP7 projects, with ARM, BSC & Bull being involved in Mont-Blanc 1, 2 and 3 projects. It will adopt a co-design approach to make sure that the hardware and system innovations are readily translated into benefits for HPC applications. This approach shall integrate architecture work (on balanced architecture and computing efficiency) together with a simulation work (to feed and validate the architecture studies) and work on the needed software ecosystem.

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