

[Inicio](#) > Combining Error Detection and Transactional Memory for Energy-efficient Computing below Safe Operation Margins

[Combining Error Detection and Transactional Memory for Energy-efficient Computing below Safe Operation Margins](#)

Authors: [Yalcin, Gulay](#) / [Sobe, Anita](#) / [Voronin, Alexey](#) / [Wamhoff, Jons-Tobias](#) / [Harmanci, Derin](#) / [Cristal, Adrián](#) / [Unsal, Osman](#) / [Felber, Pascal](#) / [Fetzer, Christof](#)

Teams: [Computer Architecture For Parallel Paradigms](#)

Publication: 22nd Euromicro International Conference on Parallel, Distributed, and Network-Based Processing

Place Published: Turin, Italy

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

Source URL (retrieved on 15 Mayo 2021 - 07:10): <https://www.bsc.es/es/node/40902>