

PATC Systems Workshop: Programming MareNostrum 4

Objectives

Objectives: The objective of this course is to present to potential users the new configuration of MareNostrum and a introduction on how to use the new system (batch system, compilers, hardware, MPI, etc).Also It will provide an introduction about RES and PRACE infrastructures and how to get access to the supercomputing resources available.

Requirements

Prerequisites: Any potential user of a HPC infrastructure will be welcome

Speakers

Convener: David Vicente, User Support Manager, Operations, BSC

Lecturers: David Vicente, Javier Bartolomé, Jorge Rodríguez, Carlos Triplana, Oscar Hernandez, Félix Ramos, Cristian Morales, Francisco González, Ricard Zarco, Helena Gómez, Pablo Ródenas, Gaurav Saxena y Maicon Faria.

Learning Outcomes

The students who finish this course will know the internal architecture of the new MareNostrum, how it works, the ways to get access to this infrastructure and also some information about optimization techniques for its architecture.

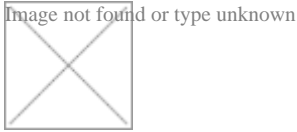
Academic Staff



Course Convener: Jorge Rodríguez

Lecturers: David Vicente, Javier Bartolomé, Jorge Rodríguez, Carlos Tripiana, Oscar Hernandez, Félix Ramos, Cristian Morales, Francisco González, Ricard Zarco, Helena Gómez, Pablo Ródenas, Gaurav Saxena y Maicon Faria.

Materials

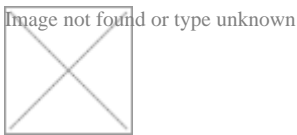


<https://www.bsc.es/support/PATC-MareNostrum4/2019>

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Further information



All PATC Courses at BSC do not charge fees.

NOTE: PLEASE BRING YOUR OWN LAPTOP.

Recommended Accomodation

Please follow [the link](#) for map of some local hotels.

CONTACT US for further details about MSc, PhD, Post Doc studies, exchanges and collaboration in education and training with BSC.

For further details about Postgraduate Studies in UPC - Barcelona School of Informatics (FiB), visit the [website](#).

Sponsors: BSC and PRACE 5IP project are funding the PATC @ BSC training events.

If you want to learn more about PRACE Project, visit the [website](#).

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

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