Inicio > Xilinx/BSC HLS and OmpSs tutorial

Xilinx/BSC HLS and OmpSs tutorial

Objectives

The tutorial will cover the main aspects of the Vivado HLS optimizations, and the OmpSs@FPGA approach. There will be a number of lab sessions based on HLS Xilinx samples for coding and optimization:

- Matrix multiplication
- RGB – YUV filter
- Discrete Cosine Transform (DCT)

The tutorial will cover the main aspects of the Vivado HLS optimizations, and the OmpSs@FPGA approach.

Requirements and other informations:

A USB Hard disk will be used with all the toolchain needed to perform the hands on. Please, test that your computer will be able to boot from a bootable Hard Disk.

Zedboards will be used in the tutorial because of two reasons:

1) we can provide up to 15 zedboards for the course and

2) it is much easier and faster to compile to them than for a bigger system like a Zynq Ultrascale+. If you can bring your own Zedboard, it would be great.

We will also provide you with a 4-GB. SD card to boot (Linux) the Zedboard with all the necessary to make the hands-on.

Further documentation will be provided before the hands-on. The registration has closed now.

Barcelona Supercomputing Center - Centro Nacional de Supercomputación