

Computer Architecture For Parallel Paradigms



For processor manufacturers, the traditional approach of increasing performance through exploiting Instruction Level Parallelism (ILP) has hit the power wall; therefore, they are shifting to the less complex approach of utilising Thread Level Parallelism (TLP). By including more processing cores on chip, total processor throughput is increased through exploiting TLP and parallel computing. However, substantial challenges lay ahead on proper hardware and architecture support for the system stack and the parallel programmed ecosystem of the future. The research group conducts research in developing hardware support to fully utilise future many-cores and to make them easier to program and debug.

Objectives

We believe that in the era of many-core chips, the software community (OS, Compiler, Programming Model, Applications) must be in the driving seat. In tandem with this new reality, the overall objective of the group is to conduct research in top-down Computer Architecture by designing hardware for software. Our overall objective is to make many-core processors easier to program. More specifically we conduct research on:

- Reliability and Fault Tolerance
- Microarchitecture for emerging applications
- Accelerators and FPGAs

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