IBM-BSC - Malleable Vector Processor Architecture and Memory

Malleable Vector Processor Architecture and Memory

This SoW supports the research effort towards the malleable higher level architecture as well as the memory optimizations. In particular, this SoW is working in four directions:

1. it is is developing a malleable instruction set which able morph and optimize itself depending on application runtime characteristics;
2. it is analyzing how to study High Bandwidth Memory (HBM) and in-memory processing using 3D stacked memory for vector processors;
3. it is developing approaches to reduce the pressure that workloads featuring massive instructions and data memory footprints put on the processor front-end and the cache hierarchy; and iv) it is developing malleable prefetching proposals to exploit all information encoded in vector memory operations to trigger prefetch requests as soon as possible and save data cache misses.

Barcelona Supercomputing Center - Centro Nacional de Supercomputación