iQ, Queue model simulation technique

iQ emulates processor elements by abstracting the implementation details into modular components composed of queue structures, delay parameters, probabilistic driven message generation and event control.

Summary

Technological improvements have led to increasingly intricate processor designs capable of achieving significant jumps in performance and energy efficiency with every new generation. Though this trend has been able to support large numbers of concurrently executing applications, the simulation tools needed for developing and validating computer architecture designs remain generally cumbersome. Finding a tool that fits the design requirements is a non-trivial feat since simulators face a trade-off of achieving either high accuracy results or tolerable simulation speed. We have developed a new simulation methodology, called iQ, which performs a rapid and accurate design space exploration to assist processor design and optimisation. The uniqueness of this tool is that it emulates the behavior of the processor components based on queuing models and statistical profiles. This approach allows a modular-based design which can be easily customised to simulate different complexity levels. iQ integrates both hardware and software into a single environment which helps to simplify the simulation and collection of analytics.

Objectives

- New simulation technique based on queue models and statistical information
• High-level simulation for design space exploration
• Fast and accurate simulations, focusing on the architectures not on the simulation tools
• Modular tool, allowing to simulate different complexity levels
• Integrated with an instruction generator

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