

Virtual BSC RS: Divide and Conquer Frontend Bottleneck

Objectives

You can watch the seminar in this [link](#).

Abstract: The frontend stalls caused by instruction and BTB misses are a significant source of performance degradation. Server processors commonly use prefetchers to mitigate the frontend bottleneck. However, next-line prefetchers, which are available in server processors, are incapable of eliminating many L1 instruction misses. Temporal prefetchers, on the other hand, eliminate most of the misses but impose significant area overhead. Finally, while BTB-directed prefetchers offer low area overhead, as they rely on the BTB content for prefetching, BTB misses stall the prefetcher, which likely leads to costly instruction misses. In this talk, I present a divide-and-conquer approach to address the frontend bottleneck. The proposal, named SN4L+Dis+BTB, imposes the same area overhead as the state-of-the-art BTB-directed prefetcher, and at the same time, outperforms it by 5% on average and up to 16%.



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Speakers

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