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## **PRACE PP: Preparatory phase for 'Computer and Data Treatment' research infrastructures in the 2006 ESFRI Roadmap (PRACE)**

### **Description**

The European Strategy Forum on Research Infrastructures (ESFRI) has identified High Performance Computing (HPC) as a strategic priority for Europe. Supercomputers are an indispensable tool to solve the most challenging problems through simulations. If Europe is to remain competitive internationally scientists and engineers must be provided with access to capability computers of leadership class.

The Partnership for Advanced Computing in Europe (PRACE) has the overall objective to prepare for the creation of a persistent pan-European HPC service, consisting of 3-5 centres, similar to the US HPC infrastructure. PRACE will be the tier-0 level of the European HPC ecosystem. It will build on the experience of the partners and use concepts and services from EC-funded projects like GEANT2 and DEISA.

The hosting centres of the planned tier-0 systems will provide the expertise, competency, and the required infrastructure for comprehensive services to meet the challenging demands of excellent users from academia and industry.

PRACE will prepare for the implementation of the infrastructure in 2009/2010 by defining and setting up a legal and organisational structure involving HPC centres, national funding agencies, and scientific user communities to ensure: adequate funding for the continued operation and periodic renewal of leadership systems; coordinated procurements; efficient use; and fair access.

In parallel, PRACE will prepare the deployment of Petaflop/s systems in 2009/2010. This includes: the procurement of prototype systems for the evaluation of software for managing the distributed infrastructure; the selection, benchmarking, and scaling of libraries and codes from major scientific user communities; the definition of technical requirements and procurement procedures; collaborations with the European IT-industry to influence the development of new technologies; and components for architectures that are promising for Petaflop/s systems to be procured after 2010.

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**Source URL (retrieved on 19 abr 2024 - 11:56):** <https://www.bsc.es/ca/research-and-development/projects/prace-pp-preparatory-phase-computer-and-data-treatment-research>