MERASA: Multi-core Execution of Hard-real-time Applications Supporting Analysability

Description

The increasing demand for functionality in current and future real-time embedded systems is driving an increase in performance of processors. However at the same time, in developing safety-related real-time embedded systems, there is a need to prove that the timing requirements are met. Multi-core processors are increasingly being considered as the solution to achieve the increased processor performance, without increasing CPU clock speeds and maintaining low chip costs, low power consumption etc. However, current trends in mainstream multi-core processor design result in processors with certainly reduced average execution times, but typically with unpredictable and unanalysable (or extremely pessimistic) worst case behaviour that deems them unusable in the domain of safety-related real-time embedded systems.

The MERASA project was developed multi-core processor designs (from 2 to 16 cores) for hard real-time embedded systems hand in hand with timing analysis techniques and tools to guarantee the analysability and predictability regarding timing of every single feature provided by the processor. Design exploration activities were performed in conjunction with the timing analysis tools. The project addressed both static WCET analysis tools (the OTAWA toolset) as well as hybrid measurement-based tools (RapiTime) and their interoperability. It also developed system-level software with predictable timing performance.

To constrain production costs and technology integration risks, the team investigated hardware based real-time scheduling solutions that empower the same multi-core processor to handle hard, soft, and non real-time tasks on different cores. The developed hardware/software techniques were evaluated by application studies from aerospace, automotive, and construction-machinery areas performed by selected industrial partners.

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