Deep-er: DEEP Extended Reach

Description

The project DEEP-ER (DEEP-Extended Reach) addresses two significant Exascale challenges: the growing gap between I/O bandwidth and compute speed, and the need to significantly improve system resiliency.

DEEP-ER will extend the Cluster-Booster architecture of the Dynamical Exascale Entry Platform (DEEP) project by a highly scalable I/O system and will implement an efficient mechanism to recover application tasks that fail due to hardware errors.

The project will leverage new memory technology to provide increased performance and power efficiency. As a result, I/O parts of HPC codes will run faster and scale up better HPC applications will be able to profit from checkpointing and task restart on large systems reducing overhead seen today. Systems that use the DEEP-ER results can run more applications increasing scientific throughput, and the loss of computational work through system failures will be substantially reduced.

DEEP-ER will build a prototype with the second generation Intel® Xeon Phi processor, a uniform high-speed interconnect across Cluster and Booster, non-volatile memory on the compute nodes, and network attached memory providing high-speed shared memory access. A highly scalable and efficient I/O system based on the Fraunhofer file system will support I/O intensive applications, using optimised I/O middleware SIONlib and EIOW. A multi-level checkpoint scheme will exploit scalable I/O and fast, non-volatile memory close to the nodes to reduce the overhead of saving state for long-running tasks. The OmpSs based DEEP programming model will govern the creation of checkpoints and restart failed tasks from the beginning or recover saved state depending on their granularity.

Seven important HPC applications will be optimised demonstrating the usability, performance and resiliency of the DEEP-ER Prototype. The applications come from different scientific and engineering areas and represent requirements of simulation-based and data-intensive HPC codes.

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Source URL (retrieved on *23 abr 2024 - 11:27*): https://www.bsc.es/ca/research-and-development/projects/deep-er-deep-extended-reach