

Published on BSC-CNS (https://www.bsc.es)

Inici > Combining Error Detection and Transactional Memory for Energy-efficient Computing below Safe **Operation Margins**

Combining Error Detection and Transactional Memory for Energyefficient Computing below Safe Operation Margins

Authors: Yalcin, Gulay / Sobe, Anita / Voronin, Alexey / Wamhoff, Jons-Tobias / Harmanci, Derin / Cristal, Adrián / Unsal, Osman / Felber, Pascal / Fetzer, Christof

Teams: Computer Architecture For Parallel Paradigms / Resilience In Distributed Systems

Publication: 22nd Euromicro International Conference on Parallel, Distributed, and Network-Based

Processing

Place Published: Turin, Italy

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

Source URL (retrieved on 19 abr 2024 - 01:45): https://www.bsc.es/ca/node/40902