Workshop on RISC-V and OpenPOWER in HPC

With the introduction of vector extensions to open instruction set architectures (ISA), the already high interest in those architectures, both academically and industrial, gained traction also in the domain of High-Performance Computing (HPC). In addition, environmental awareness and the increasing demand for computational and storage capabilities put a spotlight on the power consumption of large-scale supercomputing centers. Multiple groups published processors targeting various scenarios such as optimizations for the underlying hardware, but are also addressing specific applications and toolchains. The purpose of this workshop is to provide an overview of the advancements and challenges in open ISAs such as RISC-V and how relevant those discoveries are in the HPC domain. In addition, apart from the actual architecture, also the surrounding environment needs to be taken into consideration. Hence, the workshop will also cover topics including toolchains, applications, and simulations.

As a new and unique field, that receives more attention are topics covering security, data integrity, fault-tolerance, and reliability. Side-channel attacks on RISC-V architectures in the context of HPC seem to be an interesting addition.

Since this year would be the second year that this workshop is being held, it is an attempt to establish an event-to-be with respect to open architectures and HPC. Last year we had a long list of distinguished speakers and we are hoping to invite a healthy mix to maximize the impact of the exchange of advice, opinions, and contacts.

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