**Job Reference**

390_22_CS_EEA_RE1

**Position**

Exascale Supercomputers FPGA Engineer (RE1)

**Data de tancament**

Dilluns, 31 Octubre, 2022

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**About BSC**

The Barcelona Supercomputing Center - Centro Nacional de Supercomputación (BSC-CNS) is the leading supercomputing center in Spain. It houses MareNostrum, one of the most powerful supercomputers in Europe, and is a hosting member of the PRACE European distributed supercomputing infrastructure. The mission of BSC is to research, develop and manage information technologies in order to facilitate scientific progress. BSC combines HPC service provision and R&D into both computer and computational science (life, earth and engineering sciences) under one roof, and currently has over 770 staff from 55 countries.

Look at the BSC experience:

BSC-CNS YouTube Channel  
Let's stay connected with BSC Folks!

**Context And Mission**

BSC is looking for talented and motivated professionals with expertise in FPGA development and IP integration for a European HPC accelerator. The design is based on a RISC-V architecture. This is a project to build an FPGA-based emulator for an energy efficient Exascale system.

**Key Duties**

- Design and develop a high-performance emulation platform targeting a future Exascale Supercomputer.
- Translate/target ASIC RTL for a multi-FPGA environment.
• Design integration, logic synthesis and design optimization for area, timing and power.
• Developing front-end methodologies and tool flows.
• You will collaborate closely with design and verification engineers in active projects and perform hands-on design, writing RTL.
• Participate in system bring-up and testing.

Requirements

• Education
  • Ph.D. in Electrical Engineering or Engineering degree or equivalent level of professional experience.

• Essential Knowledge and Professional Experience
  • Design, build, test/debug and produce high-quality processor emulation platform.
  • VHDL, Verilog, and Chisel a plus.
  • Xilinx and Intel/Altera FPGA tools and processes (design, synthesis, place and route, timing closure, power analysis), including OpenCL, HLS, Chisel, and SoC tools.
  • Familiar with SystemVerilog/UVM based design verification.
  • High-speed design using advanced techniques and state-of-art devices:
    - High-end FPGAs, SOC FPGAs, memory devices, including HBM
    - IP integration
    - Standard communications and storage protocols
    - High-speed interconnect, including PCIe
  • Familiarity with Linux and device drivers.
  • Agile development and open source development, deployment, and support, including GitHub or equivalent.
  • Proficient in Microsoft Office applications or equivalent.
  • Knowledge of processor and DLP architecture and design.
  • Fluency in English is essential, Spanish is welcome.

• Competences
  • The candidate must be an effective communicator, multitask, and work well on collaborative designs.
  • Keeps abreast of technology trends.
  • Ability to think creatively.
  • Ability to work independently and make decisions.
  • Ability to take initiative, prioritize and work under set deadlines and pressure.
Conditions

- The position will be located at BSC within the Computer Sciences Department
- We offer a full-time contract, a good working environment, a highly stimulating environment with state-of-the-art infrastructure, flexible working hours, extensive training plan, tickets restaurant, private health insurance, fully support to the relocation procedures
- Duration: Open-ended contract due to technical and scientific activities linked to the project and budget duration
- Salary: we offer a competitive salary commensurate with the qualifications and experience of the candidate and according to the cost of living in Barcelona
- Starting date: ASAP

Applications procedure and process

All applications must be made through BSC website and contain:

- A full CV in English including contact details
- A Cover Letter with a statement of interest in English, including two contacts for further references - Applications without this document will not be considered

In accordance with the OTM-R principles, a gender-balanced recruitment panel is formed for every vacancy at the beginning of the process. After reviewing the content of the applications, the panel will start the interviews, with at least one technical and one administrative interview. A profile questionnaire as well as a technical exercise may be required during the process.

The panel will make a final decision and all candidates who had contacts with them will receive a feedback with details on the acceptance or rejection of their profile.

At BSC we are seeking continuous improvement in our recruitment processes, for any suggestions or feedback/complaints about our Recruitment Processes, please contact recruitment [at] bsc [dot] es.

For more information follow this link

Deadline

The vacancy will remain open until suitable candidate has been hired. Applications will be regularly reviewed and potential candidates will be contacted.

OTM-R principles for selection processes

BSC-CNS is committed to the principles of the Code of Conduct for the Recruitment of Researchers of the European Commission and the Open, Transparent and Merit-based Recruitment principles (OTM-R). This is applied for any potential candidate in all our processes, for example by creating gender-balanced recruitment panels and recognizing career breaks etc.
BSC-CNS is an equal opportunity employer committed to diversity and inclusion. We are pleased to consider all qualified applicants for employment without regard to race, color, religion, sex, sexual orientation, gender identity, national origin, age, disability or any other basis protected by applicable state or local law.
For more information follow this link
Barcelona Supercomputing Center - Centro Nacional de Supercomputación