Job Reference

315_22_CS_EEA_RE1-2-3

Position

Exascale Supercomputer ASIC/RTL Engineers (RE1-2-3)

Data de tancament

Divendres, 30 Juny, 2023

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About BSC

The Barcelona Supercomputing Center - Centro Nacional de Supercomputación (BSC-CNS) is the leading supercomputing center in Spain. It houses MareNostrum, one of the most powerful supercomputers in Europe, and is a hosting member of the PRACE European distributed supercomputing infrastructure. The mission of BSC is to research, develop and manage information technologies in order to facilitate scientific progress. BSC combines HPC service provision and R&D into both computer and computational science (life, earth and engineering sciences) under one roof, and currently has over 770 staff from 55 countries.

Look at the BSC experience:
BSC-CNS YouTube Channel
Let's stay connected with BSC Folks!

Context And Mission

BSC is looking for 5 talented and motivated professionals with expertise in ASIC design and IP integration for a European HPC accelerator. The design is based on RISC-V architecture. This is a project to build an FPGA-based emulator for an energy-efficient Exascale system.

Key Duties

- Design, including writing specifications, develop and build complex digital designs focused on scalar processors, vector units, and/or other accelerators.
- Design integration, logic synthesis and design optimization for area, timing and power.
• Develop front-end methodologies and tool flows.
• Collaborate closely with other design and verification engineers in active projects and perform hands-on design, writing RTL.
• Participate in chip bring-up and testing.

Requirements

• Education
  ○ Ph.D. in Electrical Engineering or Engineering degree or equivalent level of professional experience.

• Essential Knowledge and Professional Experience
  ○ Microprocessor architecture for modern in-order and out-of-order processor core, based on RISC-V preferred.
  ○ Knowledge of high-speed low-power design techniques. Logic synthesis and timing closure, is a plus.
  ○ System MultiProcessors related topics such as coherency and consistency.
  ○ RTL Design (Functional/Structural, Partitioning, Simulation, Regression); Tools: Modelsim, VCS.
  ○ Proficiency in Verilog/VHDL, and end-to-end design methodologies is required.
  ○ 3rd Party IP integration.
  ○ Experience in taking ASIC (gate array, library-based, and/or full custom) designs through to production is a plus.
  ○ Strong scripting/programming in csh/bash, Tcl, Python, and C/C++ is a plus.
  ○ Agile development and open source development, deployment, and support, including GitHub or equivalent.
  ○ Fluency in English is essential, Spanish is welcome.

• Competences
  ○ Effective communication, multitasking, and working well on collaborative designs
  ○ Keeping abreast on technology trends.
  ○ Ability to think creatively.
  ○ Ability to work independently and make decisions.
  ○ Ability to take initiative, prioritize and work under set deadlines and pressure.

Conditions

• The position will be located at BSC within the Computer Sciences Department
• We offer a full-time contract, a good working environment, a highly stimulating environment with state-of-the-art infrastructure, flexible working hours, extensive training plan, tickets restaurant, private health insurance, fully support to the relocation procedures
• Duration: Open-ended contract due to technical and scientific activities linked to the project and budget duration
• Salary: we offer a competitive salary commensurate with the qualifications and experience of the candidate and according to the cost of living in Barcelona
• Starting date: asap
Applications procedure and process

All applications must be made through BSC website and contain:

- A full CV in English including contact details
- A Cover Letter with a statement of interest in English, including two contacts for further references - Applications without this document will not be considered

In accordance with the OTM-R principles, a gender-balanced recruitment panel is formed for every vacancy at the beginning of the process. After reviewing the content of the applications, the panel will start the interviews, with at least one technical and one administrative interview. A profile questionnaire as well as a technical exercise may be required during the process.

The panel will make a final decision and all candidates who had contacts with them will receive a feedback with details on the acceptance or rejection of their profile.

At BSC we are seeking continuous improvement in our recruitment processes, for any suggestions or feedback/complaints about our Recruitment Processes, please contact recruitment [at] bsc [dot] es.

For more information follow this link

**Deadline**

The vacancy will remain open until suitable candidate has been hired. Applications will be regularly reviewed and potential candidates will be contacted.

**OTM-R principles for selection processes**

BSC-CNS is committed to the principles of the Code of Conduct for the Recruitment of Researchers of the European Commission and the Open, Transparent and Merit-based Recruitment principles (OTM-R). This is applied for any potential candidate in all our processes, for example by creating gender-balanced recruitment panels and recognizing career breaks etc.

BSC-CNS is an equal opportunity employer committed to diversity and inclusion. We are pleased to consider all qualified applicants for employment without regard to race, color, religion, sex, sexual orientation, gender identity, national origin, age, disability or any other basis protected by applicable state or local law.

For more information follow this link

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