Job Reference

310_19_CS_CAPP_RE23

Position

EPI Validation Engineers (RE23)

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Dissabte, 29 Febrer, 2020
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Job title: EPI Validation Engineers (RE23)

About BSC

The Barcelona Supercomputing Center - Centro Nacional de Supercomputación (BSC-CNS) is the leading supercomputing center in Spain. It houses MareNostrum, one of the most powerful supercomputers in Europe, and is a hosting member of the PRACE European distributed supercomputing infrastructure. The mission of BSC is to research, develop and manage information technologies in order to facilitate scientific progress. BSC combines HPC service provision and R&D into both computer and computational science (life, earth and engineering sciences) under one roof, and currently has over 600 staff from 49 countries.

Look at the BSC experience:
BSC-CNS YouTube Channel
Let's stay connected with BSC Folks!

Context And Mission

BSC is looking for talented and motivated professionals with expertise in Processor Design, Validation and IP integration for a European HPC accelerator in the European Processor Initiative (EPI) Project. The design is based on RISC-V architecture.

Key Duties

- You will use your design and validation expertise to actively participate in the design, build, integration and validation of complex digital systems focused on scalar processors, vector units, and/or other accelerators, including system bring up, debugging and productization.
• Design integration, logic synthesis and design optimization for area, timing and power
• Define and follow Validation Plans. Reporting and Debugging.
• Develop production and characterization test plans and specifications
• Design verification. Functional and formal verification and emulation
• Create and maintain verification & post-processing scripts for validation and debugging.
• Perform P&R parameters extraction and re-run simulations on the new implementation.
• Perform formal verification.
• Timely report on issues found, system and FU errors
• Perform bench testing to evaluate performance and measure various device parameters for design
  verification, characterization and correlation
• Participate in chip bring-up and testing
• Provide consultation to other departments performing validation activities
• Train others in the configuration, deployment, use and/or maintenance of validation software and
  workflows.
• Train others in design and development procedures applicable to development of scripting software.
• Contribute to cross-functional efforts that ensure compliance with applicable domestic and
  international regulations and standards

Requirements

• Education
  o MS degree in Electrical Engineering, Computer Engineering, or equivalent Engineering degree
    (Ph.D. preferred) with demonstrable professional experience.

• Essential Knowledge and Professional Experience
Working knowledge of Universal Verification Methodology (UVM), writing test plans, simulating, debugging, and documenting results.

Knowledge of verification concepts such as constrained randomization, coverage, and assertions.

Experience with ASIC and SOC Design Flows.

Able to create and follow validation plans/protocols/reports. Validate system requirements and verify specs. Perform Risk assessments, report results and implement remedial actions, when necessary. Provide traceability matrices for processes, systems and software / hardware validation.

Scripting ability to perform support adjustments and customization of design and Validation tools flows, including support for System Verilog, simulation and emulation, Synthesis, Place & Route and Timing Tools.

Test bench development - System Verilog UVM and C tests.

Integration/development of C tests/APIs and SW build flow.

Integration/development of UVM mailboxes and HW/SW communication components.

Integration of lower level UVM test benches.

Test plan development.

Execute tests. Analyze data, prepare reports summarizing results and statistics.

Develop and communicate expectations for quality performance, continuous improvement, process controls infrastructure for critical sustaining parts and new products.

Must be able to operate a variety of laboratory instrumentation and simulators to perform integration testing and functionality testing in hardware and software.

Power Aware test bench development and simulations.

Seamless porting between simulation/emulation/prototyping platforms.

Regression setup and debug for RTL/Gate Level Netlist/UPF PA sim/Emulation.

Coverage collection and closure.

Working with cross functional teams (DV/Arch/Design/FW) to identify coverage scope.

Interested or experienced in basic hardware debug.

Experience in RTL Design and Verification area. Experience in SoC Design Verification and HW/SW verification highly desirable.

Knowledge of low level HW/SW interaction and debug.

Experience with development of fully automated flows.

Working knowledge of Universal Verification Methodology (UVM), writing test plans, simulating, debugging, vertical test bench integration and documenting results.

Knowledge of verification concepts such as constrained randomization, coverage, and assertions.

Experience with ASIC and SOC Design Flows.

Good understanding of Processor Design and Architecture.

Excellent interpersonal, written, and verbal communication skills.

Ability to work as part of a cross-functional team according to an established timeline.

• Additional Knowledge and Professional Experience
Deep understanding of Modern in-order and out-of-order processor core and GPU designs, with expertise in one or more of the following areas: fetch, decode, branch prediction, renaming and scheduling, out-of-order execution, re-order buffer, integer, and floating-point execution, vector execution, load/store execution, caches, and memory subsystem.

Experience with one or more Instruction Set Architectures (ISAs) including RISC-V, and their implementation within in-order and out-of-order processor cores.

Strong scripting/programming in C/C++, Tcl, Python, Perl/Csh.

Strong analytic skills, familiarity with common signal processing structures (encoders, decoders, equalizers), experience with DSPs, MCUs, FPGAs, SoC, and low-power design will be considered a big plus.

Desirable: 3+ years of experience in verifying and validating hardware and software solutions.

Able to apply a risk-based approach to testing strategies, for a more efficient and targeted validation effort.

Experience integrating automated instruments with Information Management Systems (IMS).

Skilled in generating audit-ready required documentation.

Skilled in gathering software and process requirements.

Skilled in identifying root cause and complex problem-solving.

Memory subsystem with multiple banking multiple reports, crossbar connection to computing elements.

3-D, 4-D descriptor-based DMA controller with out of order responses.

Performance analysis, able to extract performance behavior through analytics.

Able to create and follow validation plans/protocols/reports. Validate system requirements and verify specs. Perform Risk assessments, report results and implement remedial actions, when necessary. Provide traceability matrices for processes, systems and software / hardware validation.

Execute tests. Analyze data, prepare reports summarizing results and statistics.

Develop and communicate expectations for quality performance, continuous improvement, process controls infrastructure for critical sustaining parts and new products.

Must be able to operate a variety of laboratory instrumentation and simulators to perform integration testing and functionality testing in hardware and software.

Provide consultation to other departments performing validation activities.

Demonstrated ability to lead cross-functional teams through the design, testing, and implementation of software-based workflows.

Demonstrated ability to lead process development, improvement, and troubleshooting projects.

Experience partnering with Quality Assurance and Information Technology to build compliant workflows, processes, and procedures.

- Competences
  - The candidate must be an effective communicator, multitask, and work well on collaborative designs.
  - Keeps abreast of technology trends
  - Ability to think creatively
  - Ability to work independently and make decisions
  - Ability to take initiative, prioritize and work under set deadlines and pressure.
  - Proficient in Microsoft Office applications or equivalent
  - Fluency in English is essential, Spanish is welcome
Conditions

- The position will be located at BSC within the [department] Department
- We offer a full-time contract, a good working environment, a highly stimulating environment with state-of-the-art infrastructure, flexible working hours, extensive training plan, tickets restaurant, private health insurance, fully support to the relocation procedures
- Duration: Temporary - [duration] renewable
- Salary: we offer a competitive salary commensurate with the qualifications and experience of the candidate and according to the cost of living in Barcelona
- Starting date: [starting-date]

Applications Procedure

All applications must include:

- A Cover Letter with a statement of interest in English, including two contacts for further references - Applications without this document will not be considered
- A full CV in English including contact details

Deadline

The vacancy will remain open until suitable candidate has been hired. Applications will be regularly reviewed and potential candidates will be contacted.

Diversity and Equal Opportunity Employment

BSC-CNS is an equal opportunity employer committed to diversity and inclusion. We are pleased to consider all qualified applicants for employment without regard to race, color, religion, sex, sexual orientation, gender identity, national origin, age, disability or any other basis protected by applicable state or local law.

This position is reserved for candidates who meet the requirements and have the legal status of disabled persons with a degree of disability equal to or greater than 33%. In case there are no applicants with disabilities that meet the requirements, the rest of the candidates without declared disability will be evaluated.

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