308_19_CS_CAPP_ RE23

Job Reference

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Position

EPI HW Design Engineers- Back end (RE23)

Data de tancament

Dissabte, 29 Febrer, 2020
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About BSC

The Barcelona Supercomputing Center - Centro Nacional de Supercomputación (BSC-CNS) is the leading supercomputing center in Spain. It houses MareNostrum, one of the most powerful supercomputers in Europe, and is a hosting member of the PRACE European distributed supercomputing infrastructure. The mission of BSC is to research, develop and manage information technologies in order to facilitate scientific progress. BSC combines HPC service provision and R&D into both computer and computational science (life, earth and engineering sciences) under one roof, and currently has over 600 staff from 49 countries.

Look at the BSC experience:
BSC-CNS YouTube Channel
Let's stay connected with BSC Folks!

Context And Mission

BSC is looking for talented and motivated professionals with expertise in Processor Design, Validation and IP integration for a European HPC accelerator in the European Processor Initiative (EPI) Project. The design is based on RISC-V architecture.

Key Duties

- You will use your design and validation expertise to design and build complex digital designs focused on scalar processors, vector units, and/or other accelerators, including writing specifications.
- Design integration, logic synthesis and design optimization for area, timing and power
- Implementation of a Processor or functional sections in RTL. Write and verify such RTL description.
- Synthesize a design given in RTL. Optimize the implementation for Area and Timing.
- Perform Place & Route and subsequent parameter extraction.
- Timing Analysis and optimization process.
- Run comparative analyses and provide analytics supporting the improvement steps taken.
- Verify correctness of the implementation. Run regressions and comparisons.
- Follow and support Validation Plans for pre and post Silicon validation. Reporting and Debugging.
- Develop and support methodologies and tool flows
- You will work closely with design and verification engineers in active projects and perform hands-on design, implementation and validation.
- Participating in chip bring-up and testing

Requirements

- Education
  - MS degree in Electrical Engineering, Computer Engineering, or equivalent Engineering degree (Ph.D. preferred) with demonstrable professional experience.

- Essential Knowledge and Professional Experience
  - Solid understanding of processor architecture and HW design. Expert knowledge of System Verilog and validation environment.
  - Working knowledge on Test & Validation techniques.
  - Proficiency in Design for Test (DFT) methodologies, Self-Test, System set up and Simulation
  - Working knowledge of the Synthesis and Place & Route methodologies.
  - Timing analysis, and feedback to design.
  - Proficiency in Verilog/ System Verilog, Chisel and end-to-end design methodologies is required
  - RTL Design (Functional/Structural, Partitioning, Simulation, Regression, Modelsim, VCS, Design Compiler, Primetime, Microprocessor Architecture, Memory Coherency)
  - Design and debug hardware and software for validation and qualification purposes
  - Perform bench testing to evaluate performance and measure various device parameters for design verification, characterization and correlation
  - 3rd Party IP integration experience

- Additional Knowledge and Professional Experience
○ Experience in taking ASIC (gate array, library-based, and/or full custom) designs through the
design, implementation, verification, P&R, debugging and test through to production
○ Strong proficiency in logic synthesis and timing closure
○ Strong scripting/programming in C/C++, Tcl, Python, Perl/Csh
○ Low Power Design (clock gating, power gating, power grids, Power Artist, UPF, CPF)
○ High-Speed DDR Controller (Memory Controller, CPU, SRAM & L3 Cache, x86 or ARM
  CPU/bus architecture)
○ Deep understanding of Modern in-order and out-of-order processor core and GPU designs, with
  expertise in one or more of the following areas: fetch, decode, branch prediction, renaming and
  scheduling, out-of-order execution, re-order buffer, integer, and floating-point execution, vector
  execution, load/store execution, caches, and memory subsystem
○ Experience with one or more Instruction Set Architectures (ISAs) including RISC-V, and their
  implementation within in-order and out-of-order processor cores
○ High-speed low-power design techniques.
○ SMP related topics such as coherency and consistency.
○ DLP (GPU/SIMD/Vector) ASIC Hardware development a plus
○ Physical Layer Design (PHY, USB, HDMI, DDR, MIPI)
○ SerDes Application (PHY Layer Protocol, SerDes PHY, ASIC EDA Models, Cadence
  Schematics)
○ Understanding of Digital Design for Mixed-Signal ASICS (PLL, Phase-Lock-Loop, LNA,
  OpAmp, ADC-DAC)
○ Performance analysis, able to extract performance behavior through analytics.
○ Able to create and follow validation plans/protocols/reports. Validate system requirements and
  verify specs. Perform Risk assessments, report results and implement remedial actions, when
  necessary. Provide traceability matrices for processes, systems and software / hardware
  validation.
○ Execute tests. Analyze data, prepare reports summarizing results and statistics.
○ Develop and communicate expectations for quality performance, continuous improvement,
  process controls infrastructure for critical sustaining parts and new products.
○ Must be able to operate a variety of laboratory instrumentation and simulators to perform
  integration testing and functionality testing in hardware and software.
○ Provide consultation to other departments performing validation activities.
○ Train others in the configuration, deployment, use and/or maintenance of validation software
  and workflows.
○ Contribute to cross-functional efforts that ensure compliance with applicable domestic and
  international regulations and standards.

• Competences
  ○ The candidate must be an effective communicator, able to multitask, and work well on
    collaborative designs
  ○ Keeps abreast of technology trends
  ○ Ability to think creatively
  ○ Ability to work independently and make decisions
  ○ Ability to take initiative, prioritize and work under set deadlines and pressure.
  ○ Proficient in Microsoft Office applications or equivalent.
  ○ Fluency in English is essential, Spanish is welcome.
Conditions

- The position will be located at BSC within the [department] Department
- We offer a full-time contract, a good working environment, a highly stimulating environment with state-of-the-art infrastructure, flexible working hours, extensive training plan, tickets restaurant, private health insurance, fully support to the relocation procedures
- Duration: Temporary - [duration] renewable
- Salary: we offer a competitive salary commensurate with the qualifications and experience of the candidate and according to the cost of living in Barcelona
- Starting date: [starting-date]

Applications Procedure

All applications must include:

- A Cover Letter with a statement of interest in English, including two contacts for further references - Applications without this document will not be considered
- A full CV in English including contact details

Deadline

The vacancy will remain open until suitable candidate has been hired. Applications will be regularly reviewed and potential candidates will be contacted.

Diversity and Equal Opportunity Employment

BSC-CNS is an equal opportunity employer committed to diversity and inclusion. We are pleased to consider all qualified applicants for employment without regard to race, color, religion, sex, sexual orientation, gender identity, national origin, age, disability or any other basis protected by applicable state or local law.
This position is reserved for candidates who meet the requirements and have the legal status of disabled persons with a degree of disability equal to or greater than 33%. In case there are no applicants with disabilities that meet the requirements, the rest of the candidates without declared disability will be evaluated.