267_21_CS_HPDA_RE3-4

Job Reference

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Position

ASIC engineer for an out-of-order processor and accelerators (RE3/RE4)

Data de tancament

Divendres, 31 Desembre, 2021

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About BSC

The Barcelona Supercomputing Center - Centro Nacional de Supercomputación (BSC-CNS) is the leading supercomputing center in Spain. It houses MareNostrum, one of the most powerful supercomputers in Europe, and is a hosting member of the PRACE European distributed supercomputing infrastructure. The mission of BSC is to research, develop and manage information technologies in order to facilitate scientific progress. BSC combines HPC service provision and R&D into both computer and computational science (life, earth and engineering sciences) under one roof, and currently has over 700 staff from 49 countries.

Look at the BSC experience:
BSC-CNS YouTube Channel
Let's stay connected with BSC Folks!

Context And Mission

The eProcessor EuroHPC project combines open source software (SW)/hardware (HW) to deliver the first completely open source European full stack ecosystem based on a new RISC-V CPU, coupled to multiple diverse accelerators that target traditional HPC and extend into mixed precision workloads for High Performance Data Analytics (HPDA), (AI, ML, DL and Bioinformatics). eProcessor will be extendable (open source), energy-efficient (low power), extreme-scale (high performance), suitable for uses in HPC and embedded applications, and extensible (easy to add on-chip and/or off-chip components).

eProcessor combines cutting edge research utilizing SW/HW co-design to achieve sustained processor and system performance for (sparse and mixed-precision) HPC and HPDA workloads by combining a high
performance low power (architecture and circuit techniques) out-of-order processor core with novel, adaptive on-chip memory structures and management, as well as fault tolerance features. These software-hardware co-design solutions span the full stack from applications to runtimes, tools, OS, and the CPU and accelerators. This can only be done with a combination of SW simulation, HW emulation using FPGAs, and real ASIC prototypes that demonstrate the full stack feasibility of the hardware and software, in a modern technology node that can easily be adopted for a near-future HPC implementation.

We are seeking one talented and motivated professional with expertise in digital ASIC implementation methodologies (synthesis and place & route), targeting tapeouts in 22nm technology.

**Key Duties**

- You will use your expertise on digital implementation to provide physical information of complex digital designs: Power, Performance and Area (PPA).
- You will collaborate closely with design and verification engineers in active projects.
- You will mentor younger engineers to make them more effective and successful in their technical career.
- You will explore and implement new state of the art methodologies and design flows.
- You will generate synthesis and implementation scripts, obtaining the best PPA characteristics for different corners.
- You will define timing constraints for IP components.
- You will work closely with the project integration team, helping to handle the complete design and submitting it to the manufacturing company.
- You will lead the elaboration of technical reports and research papers.

**Requirements**

- **Education**
  - Master’s or PhD Degree in Electronic, Electrical or Computer Engineering or equivalent level of professional experience.

- **Essential Knowledge and Professional Experience**
  - Deep knowledge of the digital ASIC design flow: synthesis, timing analysis, power analysis, place & route, signoff.
  - Knowledge of and experience with industry-standard CAD tools (Cadence Genus, Innovus, etc. or equivalent Synopsys tools - Design Compiler, ICC2, etc.).
  - Scripting using Tcl.
  - Timing constraints definition in SDC.
  - Strong background on timing analysis concepts: propagation delay, setup and hold slack, clock skew, clock domains and synchronization between domains.
  - Familiarity with the state of the art in design methodologies at the physical level: floorplanning, clock tree synthesis, hierarchical timing constraints, etc.
  - Familiarity with Github/Gitlab and git-based version control system.
  - Familiarity with Linux.
  - Fluency in English is essential, Catalan or Spanish is welcome.

- **Additional Knowledge and Professional Experience**
Experience with SoC design integrating digital and analog components is a big plus.
Previous tapeout experience is a big plus.
Knowledge of processor and accelerator architecture and design is a plus.

- Competences
  - The candidate must be an effective communicator, multitask, and work well on collaborative designs.
  - Keeps abreast of technology trends.
  - Keeps up-to-date on research advances in the area of ASIC implementation.
  - Willing to learn and handle tool documentation.
  - Ability to write research and technical papers.
  - Ability to think creatively.
  - Ability to work independently and make decisions.
  - Ability to take initiative, prioritize and work under set deadlines and pressure.

Conditions

- The position will be located at BSC within the Computer Sciences Department
- We offer a full-time contract, a good working environment, a highly stimulating environment with state-of-the-art infrastructure, flexible working hours, extensive training plan, tickets restaurant, private health insurance, fully support to the relocation procedures
- Duration: Temporary - One year, extendable until end of project renewable
- Salary: we offer a competitive salary commensurate with the qualifications and experience of the candidate and according to the cost of living in Barcelona
- Starting date: As soon as possible

Applications procedure and process

All applications must be made through BSC website and contain:

- A full CV in English including contact details
- A Cover Letter with a statement of interest in English, including two contacts for further references - Applications without this document will not be considered

In accordance with the OTM-R principles, a gender-balanced recruitment panel is formed for every vacancy at the beginning of the process. After reviewing the content of the applications, the panel will start the interviews, with at least one technical and one administrative interview. A profile questionnaire as well as a technical exercise may be required during the process.

The panel will make a final decision and all candidates who had contacts with them will receive a feedback with details on the acceptance of rejection of their profile.

For more information follow [this link](#)

Deadline

The vacancy will remain open until suitable candidate has been hired. Applications will be regularly reviewed and potential candidates will be contacted.
OTM-R principles for selection processes

BSC-CNS is committed to the principles of the Code of Conduct for the Recruitment of Researchers of the European Commission and the Open, Transparent and Merit-based Recruitment principles (OTM-R). This is applied for any potential candidate in all our processes, for example by creating gender-balanced recruitment panels and recognizing career breaks etc.

BSC-CNS is an equal opportunity employer committed to diversity and inclusion. We are pleased to consider all qualified applicants for employment without regard to race, color, religion, sex, sexual orientation, gender identity, national origin, age, disability or any other basis protected by applicable state or local law.

For more information follow this link

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

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