265_19_CS_GCS_RE12

Job Reference

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Position

Exascale Supercomputer ASIC Engineers (RE12)

Data de tancament

Divendres, 31 Gener, 2020

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About BSC

The Barcelona Supercomputing Center - Centro Nacional de Supercomputación (BSC-CNS) is the leading supercomputing center in Spain. It houses MareNostrum, one of the most powerful supercomputers in Europe, and is a hosting member of the PRACE European distributed supercomputing infrastructure. The mission of BSC is to research, develop and manage information technologies in order to facilitate scientific progress. BSC combines HPC service provision and R&D into both computer and computational science (life, earth and engineering sciences) under one roof, and currently has over 600 staff from 49 countries.

Look at the BSC experience:
BSC-CNS YouTube Channel
Let's stay connected with BSC Folks!

Context And Mission

BSC is looking for talented and motivated professionals with expertise in ASIC design and IP integration for a European HPC accelerator. The design is based on RISC-V architecture. This is a NEW project to build an FPGA-based emulator for an energy-efficient Exascale system.

Key Duties

- You will use your design expertise to design and build complex digital designs focused on scalar
• Design integration, logic synthesis and design optimization for area, timing and power.
• Developing front-end methodologies and tool flows.
• You will collaborate closely with design and verification engineers in active projects and perform hands-on design, writing RTL.
• Participating in chip bring-up and testing.

Requirements

• Education
  ○ Ph.D. in Electrical Engineering or Engineering degree or equivalent level of professional experience.

• Essential Knowledge and Professional Experience
  ○ Modern in-order and out-of-order processor core and GPU designs, with expertise in one or more of the following areas: fetch, decode, branch prediction, renaming and scheduling, out-of-order execution, re-order buffer, integer, and floating-point execution, vector execution, load/store execution, caches, and memory subsystem.
  ○ Experience with one or more, including RISC-V, Instruction Set Architectures (ISAs) and their implementation within in-order and out-of-order processor cores.
  ○ High-speed low-power design techniques.
  ○ Knowledge of logic synthesis and timing closure.
  ○ SMP related topics such as coherency and consistency.
  ○ Experience in taking ASIC (gate array, library-based, and/or full custom) designs through to production.
  ○ Proficiency in Verilog/VHDL, Chisel and end-to-end design methodologies is required.
  ○ RTL Design(Functional/Structural, Partitioning, Simulation, Regression, Modelsim, VCS, Design Compiler, Primetime, Microprocessor Architecture, Memory Coherency).
  ○ Strong scripting/programming in C/C++, Tcl, Python, Perl/Csh.
  ○ Strong analytic skills, familiarity with common signal processing structures (encoders, decoders, equalizers), experience with DSPs, MCUs, FPGAs, SoC, and low-power design will be considered a big plus.
  ○ Low Power Design (clock gating, power gating, power grids, Power Artist, UPF, CPF).
  ○ High-Speed DDR Controller (Memory Controller, CPU, SRAM & L3 Cache, x86 or ARM CPU/bus architecture).
  ○ DLP (GPU/SIMD/Vector) ASIC Hardware development a plus.
  ○ Physical Layer Design(PHY, USB, HDMI, DDR, MIPI).
  ○ Complex state machine design.
  ○ Memory subsystem with multiple banking multiple reports, crossbar connection to computing elements.
  ○ 3-D, 4-D descriptor-based DMA controller with out of order responses.
  ○ 3rd Party IP integration experience.
  ○ Agile development and open source development, deployment, and support, including GitHub or equivalent.
  ○ Proficient in Microsoft Office applications or equivalent.
  ○ Fluency in English is essential, Spanish is welcome.
• Competences
  o Effective communication, multitasking, and working well on collaborative designs
  o Keeping abreast on technology trends.
  o Ability to think creatively.
  o Ability to work independently and make decisions.
  o Ability to take initiative, prioritize and work under set deadlines and pressure.

Conditions

• The position will be located at BSC within the Computer Sciences Department
• We offer a full-time contract, a good working environment, a highly stimulating environment with state-of-the-art infrastructure, flexible working hours, extensive training plan, tickets restaurant, private health insurance, fully support to the relocation procedures
• Duration: Temporary - 2 - 3 years renewable
• Salary: we offer a competitive salary commensurate with the qualifications and experience of the candidate and according to the cost of living in Barcelona
• Starting date: ASAP

Applications Procedure

All applications must include:

• A Cover Letter with a statement of interest in English, including two contacts for further references - Applications without this document will not be considered
• A full CV in English including contact details

Deadline

The vacancy will remain open until suitable candidate has been hired. Applications will be regularly reviewed and potential candidates will be contacted.

Diversity and Equal Opportunity Employment

BSC-CNS is an equal opportunity employer committed to diversity and inclusion. We are pleased to consider all qualified applicants for employment without regard to race, color, religion, sex, sexual orientation, gender identity, national origin, age, disability or any other basis protected by applicable state or local law.  
This position is reserved for candidates who meet the requirements and have the legal status of disabled persons with a degree of disability equal to or greater than 33%. In case there are no applicants with disabilities that meet the requirements, the rest of the candidates without declared disability will be evaluated.