260_19_CS_GCS_RE12

Job Reference

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Position

Exascale Supercomputers Design Verification Engineers (RE12)

Data de tancament

Divendres, 31 Gener, 2020
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Job title: Exascale Supercomputers Design Verification Engineers (RE12)

About BSC

The Barcelona Supercomputing Center - Centro Nacional de Supercomputación (BSC-CNS) is the leading supercomputing center in Spain. It houses MareNostrum, one of the most powerful supercomputers in Europe, and is a hosting member of the PRACE European distributed supercomputing infrastructure. The mission of BSC is to research, develop and manage information technologies in order to facilitate scientific progress. BSC combines HPC service provision and R&D into both computer and computational science (life, earth and engineering sciences) under one roof, and currently has over 600 staff from 49 countries.

Look at the BSC experience:
BSC-CNS YouTube Channel
Let's stay connected with BSC Folks!

Context And Mission

BSC is looking for talented and motivated professionals with expertise in RTL Design Verification targeting ASICs and FPGAs for a European HPC accelerator. The design is based on RISC-V architecture. This is a NEW project to build an FPGA-based emulator for an energy-efficient Exascale system.

Key Duties

- You will use your design and verification expertise to verify complex digital designs.
- You will collaborate closely with design and verification engineers in active projects and perform hands-on verification.
- Using your UVM, SystemVerilog and problem-solving skills, you will build efficient and effective verification environments that exercise processor designs through their corner-cases and expose all types of bugs.
- You will be responsible for the full life cycle of verification, from verification planning to test execution, to collecting and closing coverage.

Requirements

- **Education**
  - Ph.D. in Electrical Engineering or Engineering degree or equivalent level of professional experience.

- **Essential Knowledge and Professional Experience**
  - Experienced with the full verification life cycle from test planning to signoff.
  - Knowledge of and experience with industry-standard simulators (Model/QuestaSim, VCS, etc.), revision control systems and regression systems.
  - Experienced in all latest DV methodologies: Formal Verification, System Verilog and UVM, Assembly/C-based Verification, Low power Verification using UPF/CPF.
  - Experienced in developing a DV plan based on Functional Specification, create and build the necessary verification test bench/infrastructure, develop tests and verify design.
  - Strong debugging skills and able to work with design engineers to deliver functionally correct design blocks.
  - Familiar with RTL coding using Verilog and overall design flow from Spec to Tapeout and mapping RTL to FPGAs.
  - Experience with top-level and processor-based SOC and DLP (GPU/SIMD/Vector) verification.
  - Strong scripting experience using scripting languages like Python, Perl, or Tcl.
  - Plan the verification of complex digital design blocks by fully understanding the design specification and interacting with design engineers to identify important verification scenarios.
  - Identify and write all types of coverage measures for stimulus and corner-cases.
  - Close coverage measures to identify verification holes and to show progress towards tape-out.
  - Familiarity with Linux.
  - Agile development and open source development, deployment, and support, including GitHub or equivalent.
  - Proficient in Microsoft Office applications or equivalent.
  - Knowledge of processor and GPU architecture and design.
  - Fluency in English is essential, Spanish is welcome.

- **Competences**
  - The candidate must be an effective communicator, multitask, and work well on collaborative designs.
  - Keeps abreast of technology trends.
  - Ability to think creatively.
  - Ability to work independently and make decisions.
  - Ability to take initiative, prioritize and work under set deadlines and pressure.
Conditions

- The position will be located at BSC within the Computer Sciences Department
- We offer a full-time contract, a good working environment, a highly stimulating environment with state-of-the-art infrastructure, flexible working hours, extensive training plan, tickets restaurant, private health insurance, fully support to the relocation procedures
- Duration: Temporary - 2 years renewable
- Salary: we offer a competitive salary commensurate with the qualifications and experience of the candidate and according to the cost of living in Barcelona
- Starting date: ASAP

Applications Procedure

All applications must include:

- A Cover Letter with a statement of interest in English, including two contacts for further references - Applications without this document will not be considered
- A full CV in English including contact details

Deadline

The vacancy will remain open until suitable candidate has been hired. Applications will be regularly reviewed and potential candidates will be contacted.

Diversity and Equal Opportunity Employment

BSC-CNS is an equal opportunity employer committed to diversity and inclusion. We are pleased to consider all qualified applicants for employment without regard to race, color, religion, sex, sexual orientation, gender identity, national origin, age, disability or any other basis protected by applicable state or local law.
This position is reserved for candidates who meet the requirements and have the legal status of disabled persons with a degree of disability equal to or greater than 33%. In case there are no applicants with disabilities that meet the requirements, the rest of the candidates without declared disability will be evaluated.

Barcelona Supercomputing Center - Centro Nacional de Supercomputación