**125_21_CS_CAPP_R2**

**Job Reference**

125_21_CS_CAPP_R2

**Position**

Research Engineer - Fault Tolerance and Reliability for new Computer Architecture Hardware-Software co-design (R2)

**Data de tancament**

Dimarts, 30 Novembre, 2021

**Reference:** 125_21_CS_CAPP_R2

**Job title:** Research Engineer - Fault Tolerance and Reliability for new Computer Architecture Hardware-Software co-design (R2)

**About BSC**

The Barcelona Supercomputing Center - Centro Nacional de Supercomputación (BSC-CNS) is the leading supercomputing center in Spain. It houses MareNostrum, one of the most powerful supercomputers in Europe, and is a hosting member of the PRACE European distributed supercomputing infrastructure. The mission of BSC is to research, develop and manage information technologies in order to facilitate scientific progress. BSC combines HPC service provision and R&D into both computer and computational science (life, earth and engineering sciences) under one roof, and currently has over 700 staff from 49 countries.

Look at the BSC experience:

[BSC-CNS YouTube Channel](https://www.youtube.com)

Let's stay connected with BSC Folks!

**Context And Mission**

BSC is seeking a Research Engineer to work in an exciting research project in the topic of developing fault tolerance capabilities for a new RISC-V processor. The reliability techniques developed would involve working both at the hardware as well as the software level. In particular we target to demonstrate reliability strategies for AI applications. A Ph.D. student could also be considered if the candidate has a strong background in computer fault tolerance and resilience.
Key Duties

- Develop runtime support for application-level checkpointing and automate recovery
- Develop techniques handling heterogeneous hardware, checkpointing both CPUs and FPGAs, as well as leveraging 3D stack memory
- Develop a library API that is able to checkpoint scientific applications, as well as deep learning frameworks
- Protect the critical processor structures, such as L1 Data and Instruction caches, L2 cache, TLB and register files with distinct error detection functionality (parity or lightweight ECC) according to their vulnerability and the target FIT rates for each structure
- Writing high-quality technical reports and papers.

Requirements

- Education
  - Master in Computer Science or Computer Engineering

- Essential Knowledge and Professional Experience
  - Previous hardware design experience at RTL level
  - High-speed low-power fault-tolerant digital design techniques
  - Understanding of computer architecture, preferably in high performance computing, processor micro-architecture, memory subsystem, storage
  - Knowledge of basic fault tolerance strategies such as checkpoint restart and error correcting codes
  - Experience with parallel and distributed applications (MPI+openMP)
  - Knowledge with continuous integration systems, and good coding practices

- Competences
  - Ability to work independently.
  - Ability to establish and develop research collaborations with external stakeholders.
  - Ability to present ideas and results in a precise and succinct way.

Conditions

- The position will be located at BSC within the Computer Sciences Department
- We offer a full-time contract, a good working environment, a highly stimulating environment with state-of-the-art infrastructure, flexible working hours, extensive training plan, tickets restaurant, private health insurance, fully support to the relocation procedures
- Duration: Temporary - 2 years renewable
- Salary: we offer a competitive salary commensurate with the qualifications and experience of the candidate and according to the cost of living in Barcelona
- Starting date: asap
Applications procedure and process

All applications must be made through BSC website and contain:

- A full CV in English including contact details
- A Cover Letter with a statement of interest in English, including two contacts for further references - Applications without this document will not be considered

In accordance with the OTM-R principles, a gender-balanced recruitment panel is formed for every vacancy at the beginning of the process. After reviewing the content of the applications, the panel will start the interviews, with at least one technical and one administrative interview. A profile questionnaire as well as a technical exercise may be required during the process.

The panel will make a final decision and all candidates who had contacts with them will receive a feedback with details on the acceptance of rejection of their profile.

For more information follow this link

Deadline

The vacancy will remain open until suitable candidate has been hired. Applications will be regularly reviewed and potential candidates will be contacted.

OTM-R principles for selection processes

BSC-CNS is committed to the principles of the Code of Conduct for the Recruitment of Researchers of the European Commission and the Open, Transparent and Merit-based Recruitment principles (OTM-R). This is applied for any potential candidate in all our processes, for example by creating gender-balanced recruitment panels and recognizing career breaks etc.

BSC-CNS is an equal opportunity employer committed to diversity and inclusion. We are pleased to consider all qualified applicants for employment without regard to race, color, religion, sex, sexual orientation, gender identity, national origin, age, disability or any other basis protected by applicable state or local law.

For more information follow this link

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

Source URL (retrieved on 13 nov 2021 - 16:02): https://www.bsc.es/ca/join-us/job-opportunities/12521escappr2