11_CS_CAPP_R1

Job Reference

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Position

PhD student in Fault-tolerance and low-power computing for heterogeneous hardware R1

Data de tancament

Dissabte, 31 Març, 2018

About BSC

BSC-CNS (Barcelona Supercomputing Center – Centro Nacional de Supercomputación) is the National Supercomputing Facility in Spain and manages MareNostrum, one of the most powerful supercomputers in Europe. The mission of BSC-CNS is to investigate, develop and manage information technology in order to facilitate scientific progress. With this aim, special dedication has been taken to areas such as Computer Sciences, Life Sciences, Earth Sciences and Computational Applications in Science and Engineering.

Look at the BSC experience:

BSC-CNS YouTube Channel

BSC-CNS Corporate Video

Let's stay connected with BSC Folks!

Context and Mission of the role
The Computer Architecture for Parallel Paradigms group at BSC is seeking a motivated and bright PhD student researcher to work on solving the reliability challenges for heterogeneous hardware including operating in a degraded energy-efficient mode for heterogeneous hardware composed of CPUs, GPUs and FPGAs. The student researcher will work on building fault-tolerance solutions that leverage in-memory or multi-level checkpoint-restart for emerging heterogeneous hardware with special emphasis on CPUs and FPGAs. The work will be primarily on the programming model and runtime levels of the software stack. The student researcher will use various BSC-maintained resilience tools (the OmpSs resilience branch, FTI multi-level checkpoint-restart library) in his/her daily research. Ideally, the candidate will have FPGA programming skills, with previous experience developing low-energy software optimizations a plus.

The candidate will participate in the 3-year Legato European H2020 project, giving support to the trainings of the project, and will also participate in the dissemination of the work, through conference and journal publications.

**Responsibilities**

- Research to extend several resilience libraries developed at BSC (OmpSs, FTI) to run efficiently for heterogeneous hardware composed of CPU-FPGA platforms.
- Development of recovery mechanisms in the runtime from errors incurred due to extremely low-voltage operation for FPGAs.
- Integration of the resilience techniques developed on the project platform composed of CPU-GPU-FPGAs.
- Participate in project meetings, trainings and deliverables
- Participate in group publications

**Requirements**

- **Education**
  - B.S. AND Master in Computer Science or Engineering, graduation at top of class is a plus.

- **Knowledge and professional experience**
  1. Fluency in English (both verbal and written) is a must.
  2. Excellent computing skills in programming languages (C/C++, Phyton), and experience with Linux environments (Perl, Bash). Solid background in parallel computing including programming models, runtimes, and tools.
  4. Familiar with FPGA architecture and experience with its development using verilog/vhdl and High Level Synthesis (HLS) tools such as Bluespec, Vivado, MaxJcompiler.
  5. Capacity to interact and build strong relations with the team and project partners.

**Competences**

- Excellence in English is fundamental.
- Excellent written and verbal communication skills.
- Ability to take initiative, prioritize and work under set deadlines and pressure.
- Ability to work independently and in a team.
Conditions

- The position will be located at BSC within the Computer Sciences department in collaboration with the specific project coordinator. The contract will initially be for one year. The expected project/PhD duration will be three years.

Applications Procedure

All applications must be done through the BSC website:

https://www.bsc.es/join-us/fellowships

Including:

1. Motivation letter and a statement of interest, including two recommendation letters or contacts.
2. A full CV including contact details.

Diversity and Equal Opportunity Employment

BSC-CNS is an equal opportunity employer committed to diversity and inclusion. We are pleased to consider all qualified applicants for employment without regard to race, color, religion, sex, sexual orientation, gender identity, national origin, age, disability or any other basis protected by applicable state or local law.

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