10_CS_RAA_R1

Job Reference

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Position

PhD Student to work on the Mont-Blanc 2020 Project

Data de tancament

Dissabte, 31 Març, 2018

About BSC

BSC-CNS (Barcelona Supercomputing Center – Centro Nacional de Supercomputación) is the National Supercomputing Facility in Spain and manages MareNostrum, one of the most powerful supercomputers in Europe. The mission of BSC-CNS is to investigate, develop and manage information technology in order to facilitate scientific progress. With this aim, special dedication has been taken to areas such as Computer Sciences, Life Sciences, Earth Sciences and Computational Applications in Science and Engineering.

Look at the BSC experience:

BSC-CNS YouTube Channel

BSC-CNS Corporate Video

Let's stay connected with BSC Folks!

Context and Mission of the role

Applications are invited for Master and PhD student positions in High Performance Computing (HPC) architectures at the Barcelona Supercomputing Center (BSC-CNS). We are offering PhD student positions for a period of 3 years (with possibility of extension) in the context of the H2020-funded project Mont-Blanc 2020 (MB2020).

MB2020 is a 3-year project with a 10 million euros budget funded by the European Commission under the Horizon2020 program. The main objective is to design the next generation of industrial processors for Big Data and High Performance Computing. The Mont-Blanc 2020 consortium is lead by Bull (Atos group) and also includes arm, BSC, CEA, Jülich, Kalray, and SemiDynamics (http://montblanc-project.eu/).
The MB2020 project intends to pave the way to the future low-power European processor for Exascale. To improve the economic sustainability of the processor generations that will result from the MB2020 effort, the project includes the analysis of the requirements of other markets. The project’s strategy based on modular packaging would make it possible to create a family of SoCs targeting different markets, such as “embedded HPC” for autonomous driving. The project’s actual objectives are to:

- define a low-power System-on-Chip architecture targeting Exascale;
- implement new critical building blocks (IPs) and provide a blueprint for its first generation implementation on an FPGA;
- deliver initial proof-of-concept demonstration of its critical components on real life applications;
- explore the reuse of the building blocks to serve other markets than HPC, with methodologies enabling a better time-predictability, especially for mixed-critical applications where guaranteed execution & response times are crucial.

**Requirements**

- Bachelor or M.Sc. in Computer Science (or expected to graduate in the current course).
- Computer Architecture: microarchitecture, resource sharing in multicores, cache hierarchy
- Operating Systems: Linux, scripting, OS scheduler
- Performance Analysis and Tuning of parallel applications
- Programming: C/C++, VHDL/Verilog, Assembler, Open MP/MPI, CUDA, etc.

**Competences**

- Ability to take initiative, prioritize and work under set deadlines pressure
- Ability to work independently and in a team
- Capacity to interact and build strong relations with other research groups
- Excellent written and verbal communication skills in English

**Conditions**

- A competitive salary will be provided, matched to the cost of living in Barcelona, depending on the value of the candidate

**Applications Procedure**

All applications must be done through the BSC website:

https://www.bsc.es/join-us/fellowships

Including:

1. Motivation letter and a statement of interest, including two optional recommendation letters or contacts.
2. A full CV including contact details, including BSc and MSc grades.

**Diversity and Equal Opportunity Employment**

BSC-CNS is an equal opportunity employer committed to diversity and inclusion. We are pleased to consider all qualified applicants for employment without regard to race, color, religion, sex, sexual orientation, gender identity, national origin, age, disability or any other basis protected by applicable state or local law.

Barcelona Supercomputing Center - Centro Nacional de Supercomputación