

Computer Architecture - Operating Systems (CAOS)



Multi-core and/or multi-threaded architectures are monopolising the market, from embedded systems to supercomputers. However, achieving high performance with multicore is a complex task: as the number of cores per chip and/or the number of hardware threads per core continue to increase, new challenges arise in terms of scheduling, power, temperature, scalability, analysability, design complexity, efficiency, throughput, heterogeneity, and so on.

Performance is not the only important metric anymore, and new metrics (such as security, power, total throughput, Quality of Service) are becoming more and more important. It seems clear that neither the hardware nor the software alone can achieve the desired performance and, at the same time, be compliant with these constraints.

The answer to these new challenges comes from hardware-software co-design. Computer Architectures and System Software should interact through a well-defined interface, exchanging run-time information, monitoring application progress and needs, and enforcing resource management.

Objectives

The CAOS research group carries out research mainly on real time and high performance computing with the following objectives:

1. Deploying time-analysable and low-power processor designs for the real-time arena
2. Proposing complexity-effective, low-power processor architectures with special emphasis on multicore/multithreaded architectures, and in particular in on-chip resources for high-performance and

real-time domains

3. Developing tools that allow the evaluation of different alternatives of hardware and software. The use of powerful and trustable simulation tools allows us to make design space explorations and, hence, fair comparisons between different hardware/software designs
4. Developing methodologies to fairly evaluate different processor designs. Understanding the bottlenecks of current processors is a key factor to make proposals that are of interest to industry.
5. Designing and implementing power- and temperature- aware OS solutions for real time and high performance systems (scheduling, load balancing).
6. Improving the interaction between hardware (processor) and software (operating system and run time environment).
7. Facilitating the certification of critical real-time embedded systems against safety standards, both in terms of timing and functional correctness.
8. Developing new parallel programming models and run-time systems applicable to both computing domains, i.e. high performance computing (HPC) and real-time embedded computing (EC), to exploit the performance opportunities of the newest many-core processor architectures and provide timing guarantees.

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Source URL (retrieved on 22 ago 2019 - 13:31): <https://www.bsc.es/ca/discover-bsc/organisation/scientific-structure/computer-architecture-operating-systems-caos>