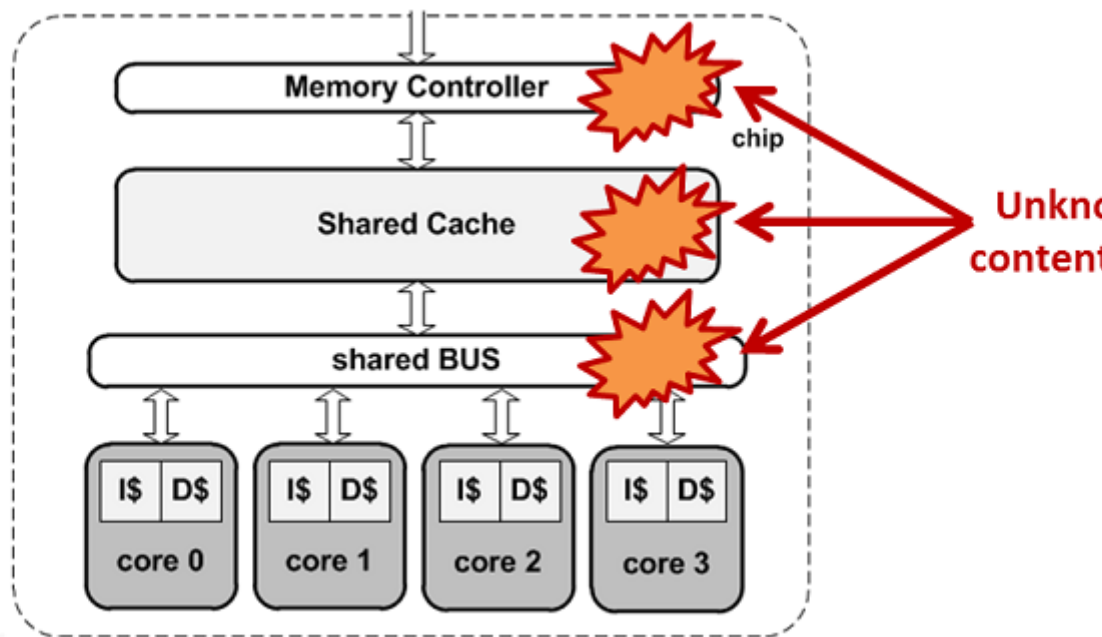# COTS multicore real-time systems

We develop new methods to derive reliable Worst-Case Execution Time (WCET) bounds for programs running in Commercial-off-the-shelf (COTS) multicore processors with unknown interference in the access to hardware shared resources.

Summary

There is an increasing need for performance in safety-related real-time systems (avionics, automotive, space, etc.) to keep the competitive edge by, for instance, developing unmanned vehicles. Such performance can only be attained realistically by using multicore processors, but due to the limited demand of this market, high-performance time-predictable multicore processors are often unavailable for many industries, which can neither afford designing their own processors. Therefore, COTS multicores are the only choice at hand in the short term.

Unfortunately, timing analyses capable to derive reliable and tight WCET estimates on top of COTS multicores are not yet sufficiently mature due to the difficulties to obtain information about the internal design of shared resources in those processors and to derive such information empirically through measurements. Contention in the access to hardware shared resources is the main concern since it typically depends on the behavior of not-yet developed software that will be running in other cores. This poses a difficult challenge in front of safety-related industry since they cannot renounce the performance of COTS multicores, but need to obtain sufficient empirical evidence (in this case timing information) within limited

time and budget constraints to certify their products against the corresponding safety standards

Objectives

In this research front we pursue the following objectives:

1. Develop practical measurement-based methods to determine the maximum contention that can be experienced by any request in the access to any hardware shared resource in a COTS multicore.
2. Devise timing analysis methods that, based on the worst-case per-request contention, can deliver reliable and tight WCET estimates for safety-related real-time tasks running on top of COTS multicores.
3. Investigate new early-design stage timing analysis methods to properly design safety-related real-time systems even before hardware and software are completely developed.

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